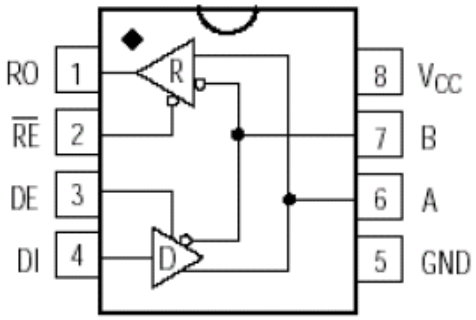
High ESD-Protected, Fail-Safe, Slew-Rate-Limited RS-485 Transceivers

General Description

The BL3085B is a half-duplex RS-485 transceiver with ±18kV IEC 61000-4-2 contact discharge protection. The BL3085B contains one driver and one receiver. The device features fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output will be logic high even if all transmitters on a terminated bus are disabled. The BL3085B features reduced slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 250kbps. The BL3085B has a 1/8 unit load receiver input impedance that allows up to 256 transceivers on the bus.

Configuration



Functional Block of BL3085B

Applications

- RS-485 Communications
- Level Translators
- Transceivers for EMI-Sensitive Applications
- Industrial Control Local Area Networks
- Energy Meter Networks
- Lighting Systems

Pin Function Description

Pin Number	Name	Function
1	RO	Receiver Output.
2	/RE	Receiver Output Enable. /RE is low to enable the Receiver; /RE is high to disable the Receiver.
3	DE	Driver Output Enable: DE is high to enable the Driver; DE is low to disable the Driver.
4	DI	Driver Input
5	GND	Ground.
6	A	Non-inverting Receiver Input and Non-inverting Driver Output.
7	B	Inverting Receiver Input and Inverting Driver Output.
8	V_{CC}	Power Supply.

Function Table

Transmitting				
Inputs			Outputs	
/RE	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown	

Receiving			
Inputs		Outputs	
/RE	DE	A-B	RO
0	X	≥-0.05V	1
0	X	≤-0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Power Supply	V_{CC}	+7	V
Control Input Voltage	/RE, DE	-0.3 to V_{CC}+0.3	V
Transmitter Input Voltage	DI	-0.3 to V_{CC}+0.3	V
Transmitter Output Voltage	A, B	-8 to +13	V
Receiver Input Voltage	A, B	-8 to +13	V
Receiver Output Voltage	RO	-0.3 to V_{CC}+0.3	V
Operating Temperature		-40 to +85	℃

DC Electrical Characteristics

（V_{CC}=+5V±5%,TA=-40℃～+85℃，Typical Values are V_{CC}=+5V and TA＝25℃）（Note 1）

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNITS
Power Supply	Vcc		4.5		5.5	V
Driver						
Differential Driver Output(no load)	V_{OD1}	Figure 1			5	V
Differential Driver Output	V_{OD2}	Figure 1，R=27Ω	1.5			V
Change in Magnitude of Differential Output Voltage（Note 2）	ΔV_{OD}	Figure 1，R=27Ω			0.2	V
Driver Common-mode Output Voltage	V_{OC}	Figure 1，R=27Ω			3	V
Change in Magnitude of Common-Mode Voltage（Note 2）	ΔV_{OC}	Figure 1，R=27Ω			0.2	V
Input High Voltage	V_{IH1}	DE,DI,/RE	2.0			V
Input Low Voltage	V_{IL1}	DE,DI,/RE			0.8	V

DI Input Hysteresis	V_{HYS}				100		mV
Input Current(A and B)	I_{IN4}	DE=GND V_{CC}=GND or 5.25V	V_{IN}=12V			125	μA
			V_{IN}=-7V			-75	
Driver Short-Circuit Output Current	I_{OSD}	-7V≦V_{OUT}≦V_{CC}		-100			mA
		0V≦V_{OUT}≦12V				100	
Receiver							
Receiver Differential Threshold Voltage	V_{TH}	-7V≦V_{CM}≦12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}				40		mV
Receiver Output High Voltage	V_{OH}	I_O=-4mA,V_{ID}=-50mV		V_{CC}-1.5			V
Receiver Output Low Voltage	V_{OL}	I_O=4mA,V_{ID}=-200mV				0.4	V
Three-State Output Current at Receiver	I_{OZR}	0.4V≦V_O≦2.4V				±1	μA
Receiver Input Resistance	R_{IN}	-7V≦V_{CM}≦12V		96			K Ω
Receiver Output Short-Circuit Current	I_{OSR}	0V≦V_{RO}≦V_{CC}		±7		±95	mA
Supply Current							
Supply Current	I_{CC}	No load ,/RE=DI= GND or V_{CC}	DE=V_{CC}		150	600	μA
			DE=GND		185	600	μA
Supply Current in Shutdown Mode	I_{SHDN}	DE=GND, /RE=VCC，DI=V_{CC} or GND				10	μA

Note 1：All currents into the device are positive. All currents out of the device are negative. All voltages are referred to device ground unless otherwise noted.

Note 2：$\triangle V_{OD}$ and $\triangle V_{OC}$ are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Switching Characteristics

（V_{CC}=+5V±5%,TA=-40℃～+85℃，Typical values are at V_{CC}=+5V，TA＝25℃）

Parameter	Symbol	Conditions	MIN	TYP	MAX	UNITS
Driver Input to Output	T_{DPLH}	Figure 3 and 5，R_{DIFF}=54Ω C_{L1}=C_{L2}=100pF		450	800	ns
	T_{DPHL}			450	800	

Driver Output Skew $\|T_{DPLH} - T_{DPHL}\|$	T_{DSKEW}	Figure 3 and 5，R_{DIFF}=54Ω C_{L1}=C_{L2}=100pF			100	ns
Driver Rise or Fall Time	T_{DR}, T_{DF}	Figure 3 and 5，R_{DIFF}=54Ω C_{L1}=C_{L2}=100pF		150	500	ns
Maximum Data Rate	F_{MAX}		250			kbps
Driver Enable to Output High	T_{DZH}	Figure 4 and 6，C_L=100pF S2 Closed			200	ns
Driver Enable to Output Low	T_{DZL}	Figure 4 and 6，C_L=100pF S1 Closed			200	ns
Driver Disable Time from Low	T_{DLZ}	Figure 4 and 6，C_L=15pF S1 Closed			300	ns
Driver Disable Time from High	T_{DHZ}	Figure 4 and 6，C_L=15pF S2 Closed			300	ns
Receiver Input to Output	T_{RPLH} T_{RPHL}	Figure 7 and 9，$\|V_{ID}\| \geq 2.0V$；rise and fall time of VID≦15ns		450	800	ns
$\|T_{RPLH} - T_{RPHL}\|$ Differential Receiver Skew	T_{RSKD}	Figure 7 and 9，$\|V_{ID}\| \geq 2.0V$；rise and fall time of VID≦15ns		30		ns
Receiver Enable to Output Low	T_{RZL}	Figure 2 and 8，C_L=100pF S1 Closed		20	50	ns
Receiver Enable to Output High	T_{RZH}	Figure 2 and 8，C_L=100pF S2 Closed		20	50	ns
Receiver Disable Time from Low	T_{RLZ}	Figure 2 and 8，C_L=100pF S1 Closed		80	150	ns
Receiver Disable Time from High	T_{RHZ}	Figure 2 and 8，C_L=100pF S2 Closed		80	150	ns
Time to Shutdown	T_{SHDN}			50	300	ns
Driver Enable from Shutdown to Output High	$T_{DZH(SHDN)}$	Figure 4 and 6，C_L=15pF S2 Closed			200	ns
Driver Enable from Shutdown to Output Low	$T_{DZL(SHDN)}$	Figure 4 and 6，C_L=15pF S1 Closed			200	ns
Receiver Enable from Shutdown to Output High	$T_{RZH(SHDN)}$	Figure 2 and 8，C_L=100pF S2 Closed			300	ns
Receiver Enable from Shutdown to Output Low	$T_{RZL(SHDN)}$	Figure 2 and 8，C_L=100pF S1 Closed			300	ns

Test Circuits and Timing Diagrams

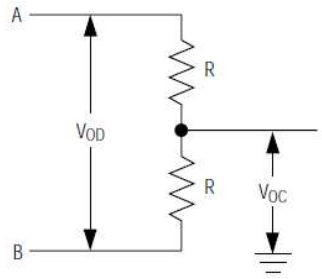


Figure 1：Driver DC Test Load

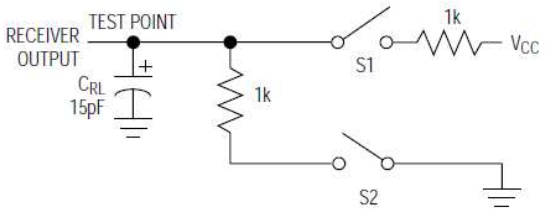


Figure 2：Receiver Enable/Disable Timing Test Load

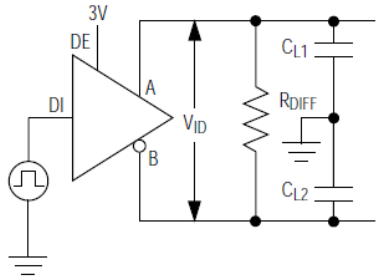


Figure 3：Driver Timing Test Circuit

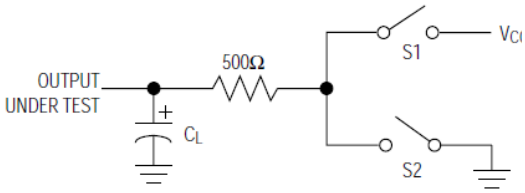


Figure 4：Driver Enable/Disable Timing test Load

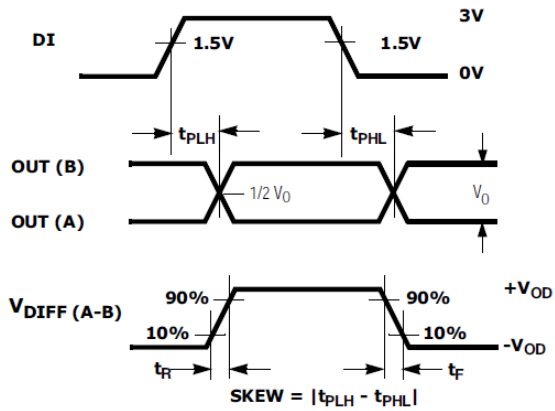


Figure 5：Driver Propagation Delays

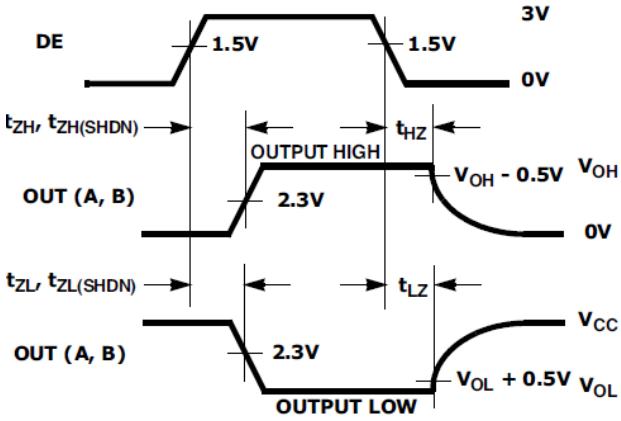


Figure 6：Driver Enable and Disable Times

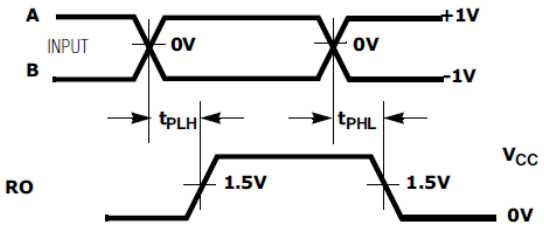


Figure 7：Receiver Propagation Delays

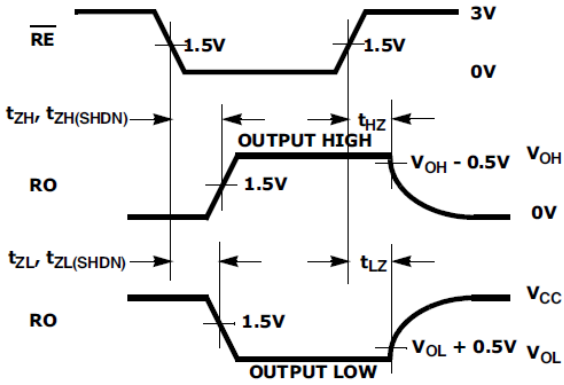


Figure 8：Receiver Enable and Disable Times

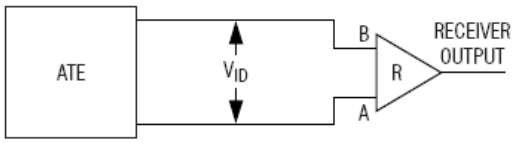
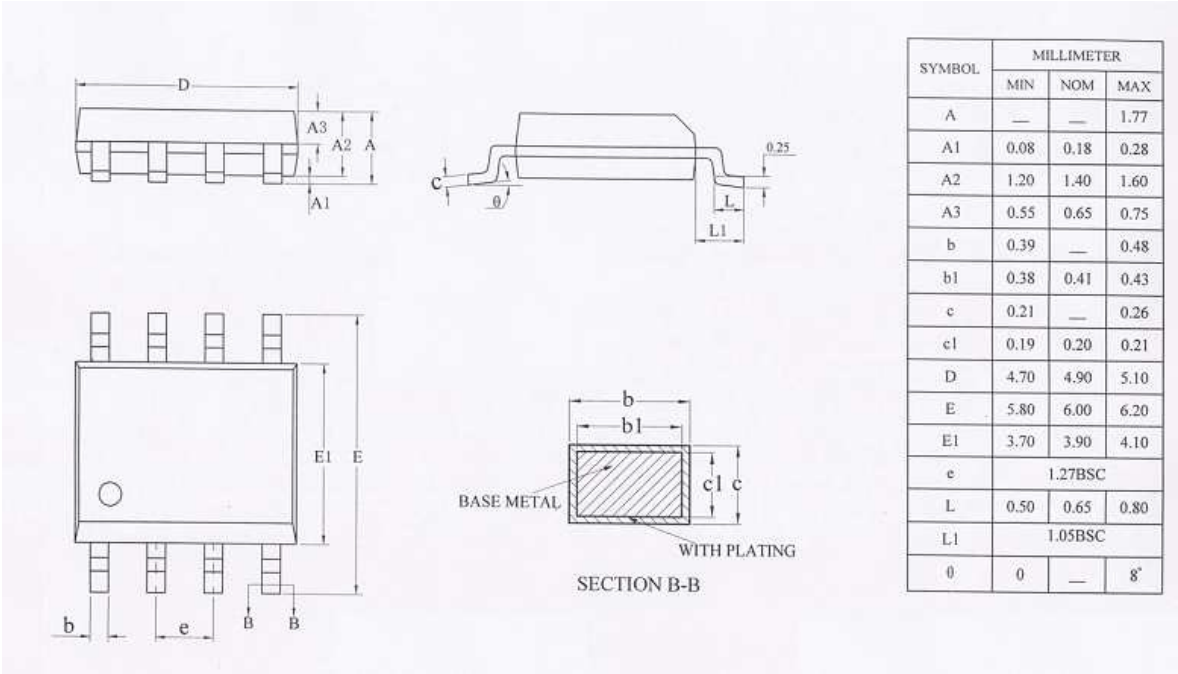


Figure 9：Receiver Propagation Delay Test Circuit

Package Information SOP8L



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.77
A1	0.08	0.18	0.28
A2	1.20	1.40	1.60
A3	0.55	0.65	0.75
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.21	—	0.26
c1	0.19	0.20	0.21
D	4.70	4.90	5.10
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	—	8°