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RTL8309N

SINGLE-CHIP 8-PORT 10/100MBPS ETHERNET SWITCH CONTROLLER

DATASHEET
Draft

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This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2012-1-10	First release.

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1. General Description

The RTL8309N is an 8-port Fast Ethernet switch controller that integrates eight MACs, and eight physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip.

The RTL8309N contains a 2K-entry address lookup table. Two 4-way associative hash algorithms avoid hash collisions and maintain forwarding performance.

Maximum packet length can be 2K bytes. Three types of independent storm filters are provided to filter packet storms, and an intelligent switch engine prevents Head-of-Line blocking problems.

The RTL8309N supports 16 VLAN groups. These can be configured as port-based VLANs and/or 802.1Q tag-based VLANs. The RTL8309N also supports four Independent VLAN Learnings (IVLs).

The RTL8309N supports several advanced QoS functions with four-level priority queues to improve multimedia or real-time networking applications, including:

- Multi-priority assignment
- Differential queue weight with WRR and SP packet scheduling
- Port-based and queue-based rate limitation

Energy-Efficient Ethernet (EEE) supports Low Power Idle Mode. When Low Power Idle Mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

The RTL8309N provides per-port one flexible LED functions for diagnostics, with five combination modes.

A loop-detection function provides notification of network loops, the loop status can be notified by buzzer, LED or both.

To simplify the peripheral power circuit, the RTL8309N integrated one LDO regulator to generate 1.0V from a 3.3V input power which needs only one external Diode.

2. Features

Basic Switching Functions

- 8-port switch controller with transceiver for 10Base-T and 100Base-TX with:
  - 8-port 10/100M UTP
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Complies with IEEE 802.3/802.3u auto-negotiation
- Built-in high efficiency SRAM for packet buffer, with 2K-entry lookup table and two 4-way associative hash algorithms
- 2K byte maximum packet length
- Flow control fully supported:
  - Half duplex: Back pressure flow control
  - Full duplex: IEEE 802.3x flow control

Service Quality

- Supports high performance QoS function on each port:
  - Supports 4-level priority queues
  - Weighted round robin service
  - Supports strict priority
  - Input/Output port bandwidth control
  - Queue based bandwidth control
  - 1Q-based, Port-based, DSCP-based, IP address-based, and other types of priority assignments
- Supports IEEE 802.1p Traffic Re-marking

Security and Management

- Supports reserved control frame filtering
- Supports advanced storm filtering
- Optional EEPROM interface for configuration

VLAN Functions

- Supports up to 16 VLAN groups
- Flexible 802.1Q port/tag-based VLAN
- Supports four IVLs
- Leaky VLAN for unicast/multicast/broadcast/ARP packets

Power Saving Functions

- Supports Energy-Efficient Ethernet (EEE) function (IEEE 802.3az)
- Link down Power Saving Mode

Diagnostic Functions

- Supports hardware loop detection function, with LEDs to indicate the existence of a loop
- Supports cable diagnosis (RTCT function)
- LED indicators:
  - Loop status indication
  - RTCT status indication
  - LEDs blink upon reset for LED diagnostics

Other Features

- Optional MDI/MDIX auto crossover for plug-and-play
- Physical layer port Polarity Detection and Correction function

- Robust baseline wander correction for improved 100Base-TX performance
- 25MHz crystal
- Integrated LDO regulator to generate 1.0V from 3.3V via one external Diode
- Low power, 1.0/3.3V, 55nm CMOS technology
- 64-pin QFN package

3. Block Diagram

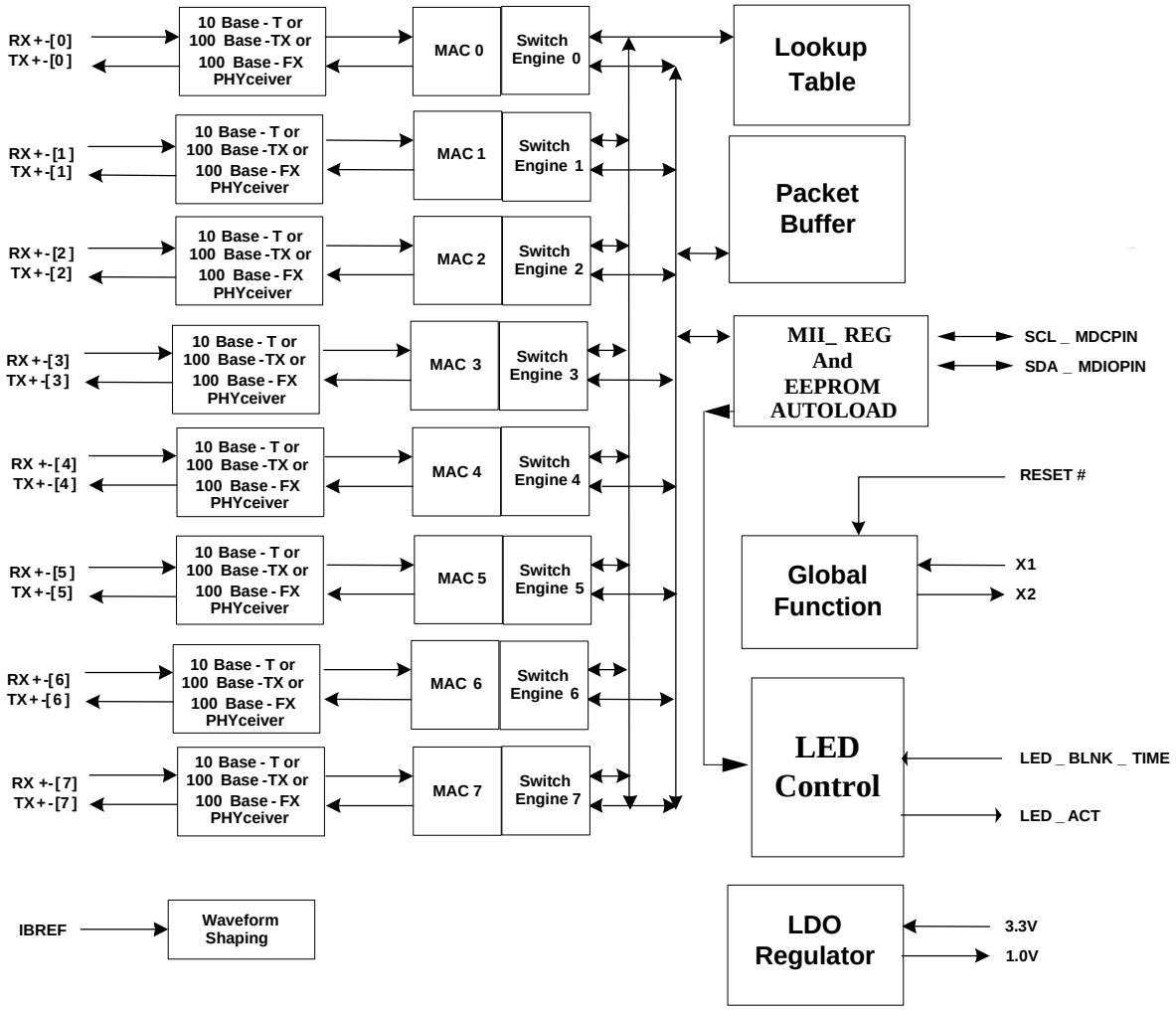


Figure 1. Block Diagram

4. Pin Assignments

4.1. Pin Assignments Diagram

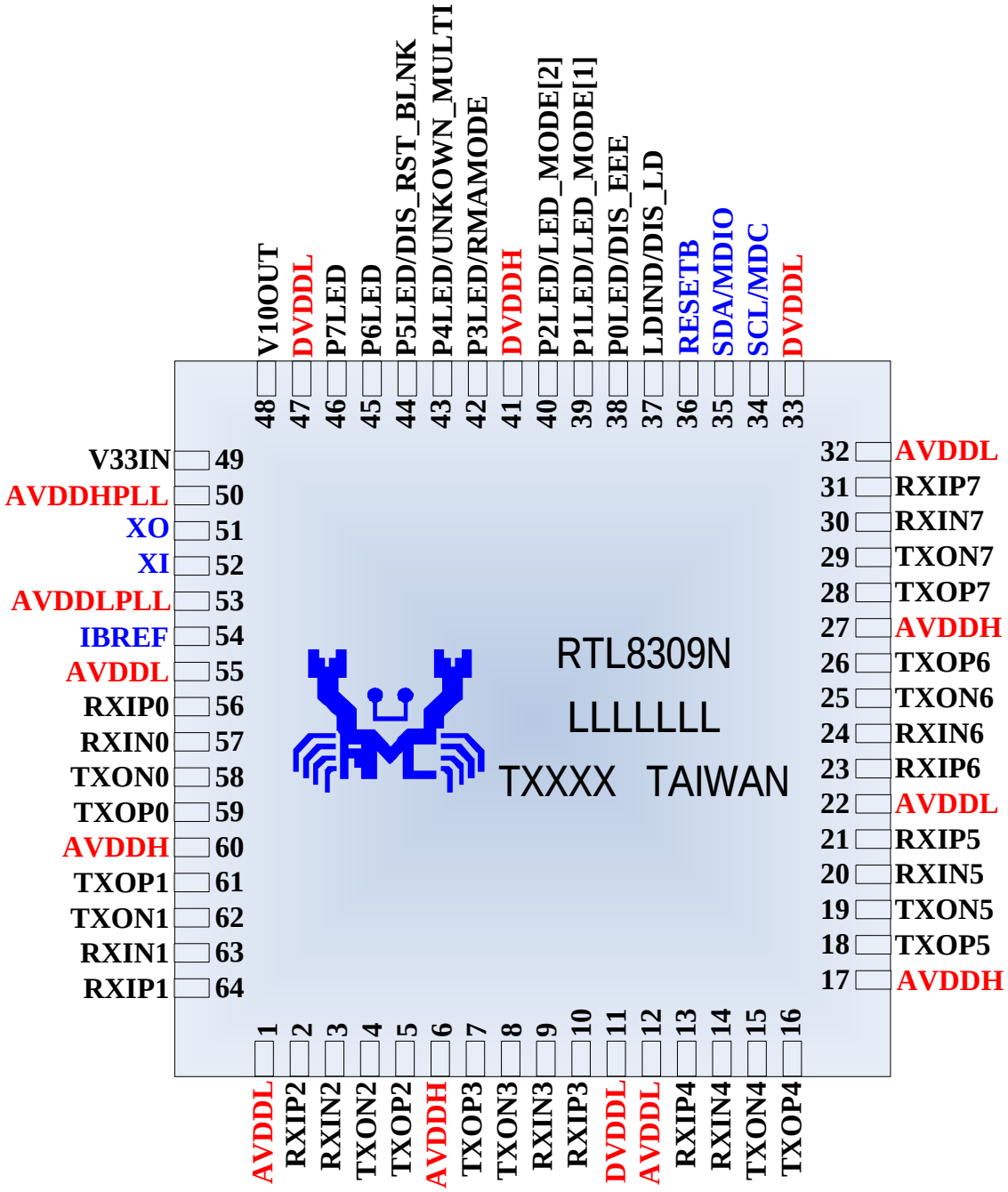


Figure 2. Pin Assignments

4.2. Package Identification

Green package is indicated by a 'G' in the location marked 'T' in 错误！未找到引用源。.

4.3. Pin Assignments Table

Upon Reset: Defined as a short time after the end of a hardware reset.
After Reset: Defined as the time after the specified 'Upon Reset' time.

I:	Input Pin	AI:	Analog Input Pin
O:	Output Pin	AO:	Analog Output Pin
I/O:	Bi-Direction Input/Output Pin	AI/O:	Analog Bi-Direction Input/Output Pin
P:	Digital Power Pin	AP:	Analog Power Pin
G:	Digital Ground Pin	AG:	Analog Ground Pin
I_{PU}:	Input Pin With Pull-Up Resistor; (Typical Value is about 75KΩ)	O_{PU}:	Output Pin With Pull-Up Resistor; (Typical Value is about 75KΩ)
I_{PD}:	Input Pin With Pull-Down Resistor; (Typical Value is about 75KΩ)	O_{PD}:	Output Pin With Pull-Down Resistor; (Typical Value is about 75KΩ)
I/O_{PU}:	I_{PU} and O_{PU}	I/O_{PD}:	I_{PD} and O_{PD}

Table 1 Pin Assignments Table

Name	Pin No.	Type
AVDDL	1	AP
RXIP[2]	2	AI/O
RXIN[2]	3	AI/O
TXON[2]	4	AI/O
TXOP[2]	5	AI/O
AVDDH	6	AP
TXOP[3]	7	AI/O
TXON[3]	8	AI/O
RXIN[3]	9	AI/O
RXIP[3]	10	AI/O
DVDDL	11	P
AVDDL	12	AP
RXIP[4]	13	AI/O
RXIN[4]	14	AI/O
TXON[4]	15	AI/O
TXOP[4]	16	AI/O
AVDDH	17	AP
TXOP[5]	18	AI/O

Name	Pin No.	Type
TXON[5]	19	AI/O
RXIN[5]	20	AI/O
RXIP[5]	21	AI/O
AVDDL	22	AP
RXIP[6]	23	AI/O
RXIN[6]	24	AI/O
TXON[6]	25	AI/O
TXOP[6]	26	AI/O
AVDDH	27	AP
TXOP[7]	28	AI/O
TXON[7]	29	AI/O
RXIN[7]	30	AI/O
RXIP[7]	31	AI/O
AVDDL	32	AP
DVDDL	33	P
SCL/MDC	34	I/O_{PU}
SDA/MDIO	35	I/O_{PU}
RESETB	36	I_{PU}

Name	Pin No.	Type
LDIND	37	I/O $_{PU}$
P0LED	38	I/O $_{PD}$
P1LED	39	I/O $_{PD}$
P2LED	40	I/O $_{PD}$
DVDDH	41	P
P3LED	42	I/O $_{PD}$
P4LED	43	I/O $_{PD}$
P5LED	44	I/O $_{PD}$
P6LED	45	I/O $_{PD}$
P7LED	46	I/O $_{PD}$
DVDDL	47	P
V10OUT	48	AO
V33IN	49	AP
AVDDHPLL	50	AP
XO	51	O
XI	52	I
AVDDLPLL	53	AP
IBREF	54	AO
AVDDL	55	AP
RXIP[0]	56	AI/O
RXIN[0]	57	AI/O
TXON[0]	58	AI/O
TXOP[0]	59	AI/O
AVDDH	60	AP
TXOP[1]	61	AI/O
TXON[1]	62	AI/O
RXIN[1]	63	AI/O
RXIP[1]	64	AI/O
E-PAD	E-PAD	G

4.4. Pin Descriptions

4.4.1. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RXIP7/RXIN7 RXIP6/RXIN6 RXIP5/RXIN5 RXIP4/RXIN4 RXIP3/RXIN3 RXIP2/RXIN2 RXIP1/RXIN1 RXIP0/RXIN0	31,30 23,24 21,20 13,14 10,9 2,3 64,63 56,57	AI/O	-	Differential Receive Data Input: Port0-7 support 10Base-T, 100Base-TX and 100Base-FX
TXOP7/TXON7 TXOP6/TXON6 TXOP5/TXON5 TXOP4/TXON4 TXOP3/TXON3 TXOP2/TXON2 TXOP1/TXON1 TXOP0/TXON0	28,29 26,25 18,19 16,15 7,8 5,4 61,62 59,58	AI/O	-	Differential Transmit Data Output: Port0-7 support 10Base-T, 100Base-TX and 100Base-FX

4.4.2. Parallel LED Pins

Table 3. Parallel LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
P0LED	38	I/O_{PD}	10	LED for Port0 status indication
P1LED	39	I/O_{PD}	10	LED for Port1 status indication
P2 LED	40	I/O_{PD}	10	LED for Port2 status indication
P3 LED	42	I/O_{PD}	10	LED for Port3 status indication
P4 LED	43	I/O_{PD}	10	LED for Port4 status indication
P5 LED	44	I/O_{PD}	10	LED for Port5 status indication

Pin Name	Pin No.	Type	Drive (mA)	Description
P6 LED	45	I/O_{PD}	10	LED for Port6 status indication
P7 LED	46	I/O_{PD}	10	LED for Port7 status indication

4.4.3. Miscellaneous Interface Pins

Table 4. Miscellaneous Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LDIND	37	I/O_{PU}	10	Loop indication used by LED and buzzer, when loop topology is happened.
SCL/MDC	34	I/O_{PU}	4	I^2C Interface Clock for EEPROM auto load when power on, and after power on, this pin is MDC/MDIO Interface Clock for access registers
SDA/MDIO	35	I/O_{PU}	4	I^2C Interface Data Input/Output for EEPROM auto load when power on, and after power on, this pin is MDC/MDIO Interface Data Input/Output for access registers.
RESETB	36	I_{PU}	-	System Pin Reset Input.
XI	52	AI	-	25MHz Crystal Clock Input. The clock tolerance is ±50ppm. When using an oscillator, this pin should be tied to ground.
XO	51	AO	-	25MHz Crystal Clock Output Pin.
IBREF	54	AO	-	Reference Resistor for PHY bandgap. A 2.49KΩ (1%) resistor should be connected between IBREF and GND.

4.4.4. Configuration Strapping Pins

Table 5. Configuration Strapping Pins

Pin Name	Pin No.	Type	Default	Description

Pin Name	Pin No.	Type	Default	Description
DISLD (LDIND)	37	I/O_{PU}	-	Disable loop detection function. 0: Enable 1: Disable (default)
DIS_EEE (P0LED)	38	I/O_{PD}	-	Disable EEE function 0: enable EEE function (default) 1: disable EEE function
LED_MODE1 (P1LED)	39	I/O_{PD}	-	LED Mode[2:1] Select. 2'b00/2'b01: Mode 0/1: Link+Act(default) 2'b10: Mode 2: Duplex 2'b11: Mode 3: Speed100+Act
LED_MODE2 (P2LED)	40	I/O_{PD}	-	LED Mode[2:1] Select. 2'b00/2'b01: Mode 0/1: Link+Act(default) 2'b10: Mode 2: Duplex 2'b11: Mode 3: Speed100+Act
RMAMODE (P3LED)	42	I/O_{PD}	-	RMA mode select: 0: Mode0 is selected (default) 01-80-c2-00-00-02 is drop and 01-80-c2-00-00-11 ~ 01-80-c2-00-00-1F, 01-80-c2-00-00-21 packet are forwarded 1: Mode1 is selected 01-80-c2-00-00-02 is forward and 01-80-c2-00-00-11 ~ 01-80-c2-00-00-1F, 01-80-c2-00-00-21 packet are dropped
UNKOWN_MULTI (P4LED)	43	I/O_{PD}	-	Enable unknown multicast data packet drop 0: forward all unknown multicast data packet (default) 1: drop all unknown multicast data packet (expect IGMP/MLD and RMA packet)
DIS_RST_BLNK (P5LED)	44	I/O_{PD}	-	Disable LED Power on Blinking: 0: enable (default) 1: disable

4.4.5. Regulator Pins

Table 6. Regulator Pins

Pin Name	Pin No.	Type	Drive (mA)	Description

Pin Name	Pin No.	Type	Drive (mA)	Description
V10OUT	48	AO	-	Switch Regulator 1.0V output.
V33IN	49	AP	-	Switch Regulator 3.3V input

4.4.6. Power and GND Pins

Table 7. Power and GND Pins

Pin Name	Pin No.	Type	Description
AVDDH	6,17,27,60	AP	Analog Power 3.3V.
AVDDL	1,12,22,32,55	AP	Analog Power 1.0V.
AVDDHPLL	50	AP	Power 3.3V for PLL.
AVDDLPLL	53	AP	Power 1.0V for PLL.
DVDDH	41	P	Digital Power 3.3V for IO Pad.
DVDDL	11,33,47	P	Digital Power 1.0V for Core Voltage.
GND	E-PAD	G	Ground for whole chip

5. Physical Layer Function Description

5.1. MDI Interface

The RTL8309N embeds 8 Fast Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 10Base-T, 100Base-TX and 100Base-FX. This interface consists of two signal pairs RXIP/RXIN, and TXOP/TXON. The MDI interface has internal termination resistors for reduced BOM cost and PCB complexity.

5.2. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

5.3. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

5.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

5.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

5.6. 100Base-FX Function

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and needs no SD+/- pins. 100Base-FX can be forced to full duplex with optional flow control ability.

Note: In compliance with IEEE 802.3u, 100Base-FX does not support Auto-Negotiation. In order to operate correctly, both sides of the connection should be set to the same flow control ability.

A scrambler is not needed in 100Base-FX. Compared to common 100Base-FX applications, the RTL8309N removes a pair of differential SD (Signal Detect) signals that provide a link monitoring function, which reduces the pin count (Realtek patent).

5.7. Auto-Negotiation for UTP Function

The RTL8309N obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8309N advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

5.8. Crossover Detection and Auto Correction Function

During the link setup phase, the RTL8309N checks whether it receives active signals on every port in order to determine if a connection can be established. RTL8309N can identify the type of connected cable and sets the port to MDI or MDIX. When switching to MDI mode, the RTL8309N uses TXOP/N as transmit pair; when switching to MDIX mode, the RTL8309N uses RXIP/N as transmit pair.

5.9. Polarity Correction Function

The RTL8309N automatically corrects polarity errors on the receiver pairs in the 10Base-T modes. In 100Base-TX mode, the polarity does not matter.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

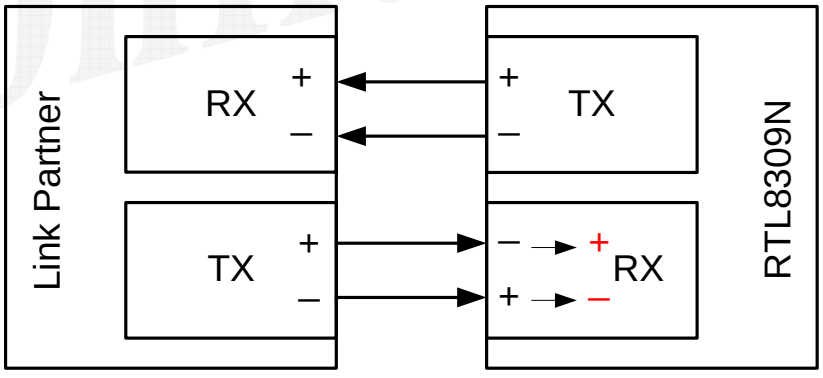


Figure 3. Conceptual Example of Polarity Correction

5.10. IEEE 802.3az Energy Efficient Ethernet Function (EEE)

The RTL8309N supports IEEE 802.3az Energy Efficient Ethernet (EEE) ability for 100Base-TX in full duplex operation, and supports 10Base-Te for 10Base-T in full/half duplex .The Energy Efficient Ethernet (EEE) operational mode combines the IEEE 802.3 Media Access Control (MAC) Sub-layer with a family of Physical Layers defined to support operation in Low Power Idle (LPI) Mode. When the port is in LPI

Mode, link partners of both sides can turn off the unnecessary TX/RX circuits to save power consumption during periods of low link utilization.

The RTL8309N EEE operational mode supports the IEEE 802.3 MAC operation at 100Mbps. In addition, the RTL8309N supports 10Mbps PHY with reduced transmit amplitude requirements in EEE operational mode. This new PHY is fully interoperable with legacy 10Base-T PHY over 100m of class D (Category 5) or better cabling.

5.11. Link Down Power Saving Function

The RTL8309N implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. A port automatically enters link down power saving mode 3 seconds after the cable is disconnected from it. Once a port enters link down power saving mode, it transmits normal link pulses on its TX and continues to monitor the RX to detect incoming signals, which might be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from link down power saving mode and operates in normal mode according to the result of the connection.

6. Switch Core Function Description

6.1. Hardware Reset and Software Reset Function

6.1.1. Hardware Reset

A hardware reset forces the RTL8309N to start the initial power-on sequence. First hardware will strap pins to give all default values when the 'RESETB' signal terminates. Next the configuration is auto-loaded from EEPROM (if EEPROM is detected), and then the complete SRAM BIST (Built-In Self Test) process is run.

6.1.2. Software Reset

The RTL8309N supports software reset to reset Switch packet buffer.

6.2. Layer 2 Learning and Forwarding Function

The RTL8309N MAC address table consists of an 2K-entry L2 hash table and a 2-entry forwarding table. The RTL8309N supports IVL (Independent VLAN Learning), SVL (Shared VLAN Learning), and IVL/SVL (Both Independent and Shared VLAN Learning).

6.2.1. Forwarding

When the VLAN egress filtering option is enabled, a received unicast frame will be forwarded to its destination port only if the destination port is in the same VLAN as the source port. If the destination port belongs to a different VLAN, the frame will be discarded.

By default the received broadcast/multicast frame will flood to VLAN member ports only, except for the source port.

IP Multicast data packets involve multicast address table lookup and forwarding operations. If the table lookup returns a hit, the data packet is forwarded to member ports according to forwarding table setting. If the IP multicast address is not stored in the address table (i.e., lookup miss), according to a 1-bit action configuration the packet is dropped or flooded.

6.2.2. Learning

The RTL8309N features a Layer2 table (2K entries). It uses a 4-way hash structure to store L2 entries. Each entry can learn in the format of L2 Unicast, and the L2 Unicast hash key is {MAC, FID}.

6.2.3. Address Table Aging

In a dynamic network topology, address aging allows the contents of the address table to always be the most recent and correct. A learned source address entry will be cleared (aged out) if it is not updated by the address learning process within an aging time period. The aging time of the RTL8309N is between 200 and 400 seconds (typical value is 300 seconds). The RTL8309N also supports a fast aging function that is used to age all dynamic entries within 1ms.

6.2.4. Layer 2 Multicast

The RTL8309N supports two IP multicast frame types: IPv4 multicast and IPv6 multicast.

The RTL8309N IGMPv1/2/3 and MLDv1/2 packets can be trapped to the CPU, to allow software to insert an IP multicast entry into the address table.

6.3. MAC Limit Function

The RTL8309N supports the capability of limiting the number of MAC addresses that are learned. The learned MAC addresses of each port, and the total learned MAC addresses of any combination of multi ports can be limited. The limit thresholds of each port can be configured independently.

There is a counter for each of the limits. The counter will be decremented if a counted MAC address ages out. Deleting or creating entries in the LUT via register setting will not affect these counters. When the

MAC limit of port(s) reached, the received packet on the corresponding port, which is not learned or is learned but is not the current ingress port, will be dropped and not be learned.

6.4. Reserved Multicast Address Handling Function

The RTL8309N supports Reserved Multicast Address (RMA) as defined in the IEEE 802.1 standard. For each RMA, the actions include: Forward, Drop, Trap or Copy to CPU. The action priority is higher than the results of a L2 Table lookup. Default actions are shown in Table 8.

Table 8. Reserved Multicast Address Default Actions

Name	Address	Default
Bridge Group Address	01-80-C2-00-00-00	Forward
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01	Drop
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02	Drop
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03	Forward
Reserved for future protocol standards	01-80-C2-00-00-04~01-80-C2-00-00-0D, 01-80-C2-00-00-0F	Drop
LLDP IEEE Std 802.1AB Link Layer Discovery Protocol Multicast Address	01-80-C2-00-00-0E	Forward
All LANs Bridge Management Group Address	01-80-C2-00-00-10	Drop
Reserved for 01-80-C2-00-00-1x	01-80-C2-00-00-11~01-80-C2-00-00-1F	Forward
GMRP	01-80-C2-00-00-20	Drop
GVRP	01-80-C2-00-00-21	Forward
Reserved for use by Multiple Registration Protocol (MRP) applications	01-80-C2-00-00-22 ~ 01-80-C2-00-00-2F	Drop
IEEE 802.1ag PDU CCM/LTM	01-80-C2-00-00-31 ~ 01-80-C2-00-00-3F	Forward

6.5. IEEE 802.3x Flow Control Function

The RTL8309N supports IEEE 802.3x full duplex flow control. If one port's receive buffer is over the pause-on threshold, a pause-on frame is sent to the link partner to stop the transmission. When the port's receive buffer drops below the pause-off threshold, it sends a pause-off frame. The pause frame format is shown in Figure 4.

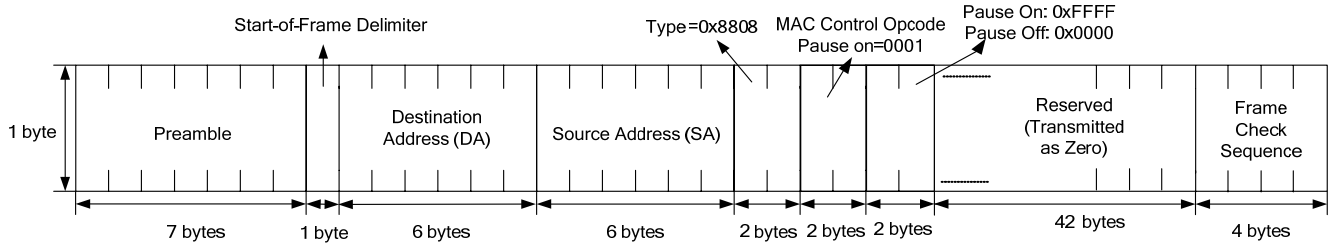


Figure 4. Tx Pause Frame Format

The RTL8309N is implemented three type flow control mechanism: output flow control, input flow control and input bandwidth control base flow control.

When RTL8309N flow control is enabled, the initial state is 'Non_Congest'. The state is monitored continuously. If a pause-on trigger condition occurs, it enters the 'Congest' state. When in the 'congest' state, it is also continuously monitored. When a pause-off trigger condition occurs it re-enters the 'Non_Congest' state. Figure 5 shows the flow control state machine.

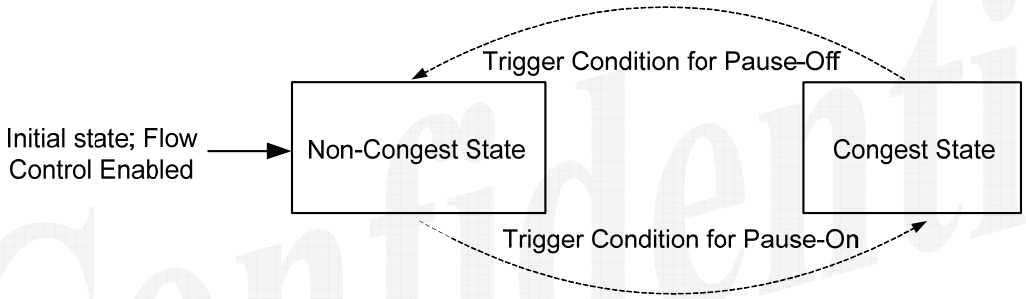


Figure 5. Flow Control State Machine

6.6. Half Duplex Backpressure Function

There are two mechanisms for half-duplex backpressure: collision-based or carrier-based.

6.6.1. Collision-Based Backpressure (Jam Mode)

If the buffer is ready to overflow, this mechanism will force a collision. When the link partner detects this collision, the transmission is rescheduled.

The Reschedule procedure is:

- The RTL83109N will drive TXEN to high and send the preamble, SFD and a 4-byte Jam signal (pattern is 0xAA). Then the RTL8309N will drive TXEN to low.
- When the link partner receives the Jam signal, it will feedback a 4-byte signal (pattern is CRC^0x01), then it will drive RXDV to low.

- The link partner waits for a random back-off time then re-sends the packet. The timing is shown in Figure 6.

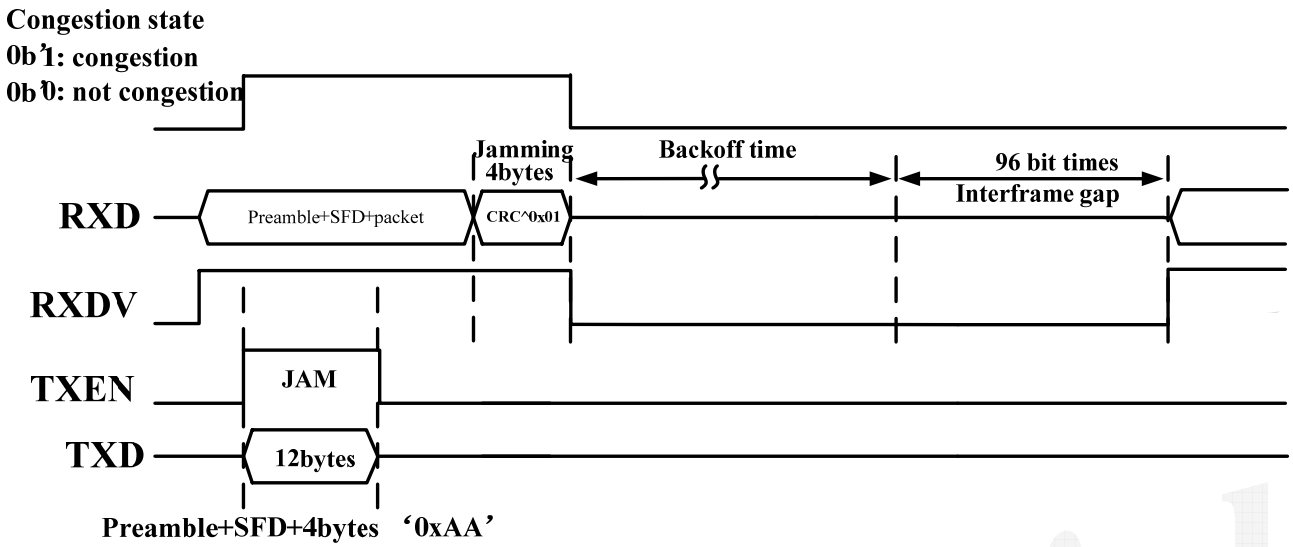


Figure 6. Collision-Based Backpressure Signal Timing

6.6.2. Carrier-Based Backpressure (Defer Mode)

If the buffer is about to overflow, this mechanism will send a 0xAA pattern to defer the other station's transmission. The RTL8309N will continuously send the defer signal until the buffer overflow is resolved.

6.7. VLAN Function

The RTL8309N supports 16 VLAN groups with the 16-entry VLAN table (see Table 9 and Table 10). These can be configured as port-based VLANs and/or IEEE 802.1Q tag-based VLANs. The RTL8309N supports IVL/SVL function, using the FID to lookup layer2 table. The contents of the VLAN table can be configured via SMI or EEPROM. Multiple ingress filtering and egress filtering options provide various VLAN admit rules for the RTL83009N. The RTL83009N also provides flexible VLAN tag insert/remove function.

Table 9. VLAN Table

Entry Index	VLAN ID	MBR	UNTAG SET	FID
VLAN Entry 0	VLAN ID A[11:0]	VLAN ID A membership [8:0]	VLAN ID A UNTAG_MSK [8:0]	FID[1:0]
VLAN Entry 1	VLAN ID B [11:0]	VLAN ID B membership [8:0]	VLAN ID B UNTAG_MSK [8:0]	FID[1:0]
……	……	……	……	……
VLAN Entry 15	VLAN ID P [11:0]	VLAN ID P membership [8:0]	VLAN ID P UNTAG_MSK [8:0]	FID[1:0]

Table 10. VLAN Entry

Field	Description	Bits
VID	The VLAN ID for search. The VID of the ingress packet will be compared with this field.	12
MBR	VLAN member port set. If the bit in this field is '1', the corresponding port is a member port of the VLAN specified by the VID field.	9
UNTAG SET	VLAN untag set. If the bit in this field is '1', the packet egressing from the corresponding port will be VLAN-untagged.	9
FID	The FID is for Layer2 table lookup.	2

6.7.1. Port-Based VLAN

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members. The RTL8309N supports VLAN indexes for each port to individually index this port to one of the 16 VLAN entry. A port that is not included in a VLAN's member set cannot transmit packets to this VLAN.

6.7.2. IEEE 802.1Q Tagged-VID Based VLAN

The RTL8309N uses a 12-bit explicit identifier in the VLAN entry to associate received packets with a VLAN tag. If the VID of a VLAN-tagged frame does not match any of the 16 VLAN entries, the RTL8309N will drop the frame if the VLAN packet trap to the CPU port function is disabled. Otherwise, the RTL8309N compares the explicit identifier in the VLAN tag with the 16 VLAN IDs to determine the VLAN association of this packet, and then forwards this packet to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

6.7.3. Insert/Remove/Replace Tag

The RTL8309N supports the VLAN Insertion/Removal/replacing action for each port. The 802.1Q VLAN tags can be inserted, removed, or replaced based on the port's setting.

6.7.4. Ingress and Egress Rules

The RTL8309N provides flexible VLAN ingress and egress rules to permit comprehensive traffic control. The RTL8309N can filter packets on ingress according to the tag condition of the packet. For a normalized VLAN application, each of the RTL8309N ports can be independently configured to:

- 'admit all frames'
- 'admit only tagged frames'
- 'admit only untagged frames'

Note: The priority tagged frame (VID=0) will be treated as an untagged frame.

The RTL8309N also can optionally discard a frame associated with a VLAN of which the ingress port is not in the member set.

For the egress filter, the RTL8309N drops the frame if this frame belongs to a VLAN but its egress port is not one of the VLAN's member ports. However, there are 5 leaky options to provide exceptions for special applications.

- 'Unicast leaky VLAN' enables inter-VLAN unicast packet forwarding. That is, if the layer 2 lookup table search has a hit, then the unicast packet will be forwarded to the egress port, ignoring the egress rule.
- 'Broadcast leaky VLAN' enables inter-VLAN broadcast packet forwarding. Packets may be flooded to all other ports, ignoring the VLAN member set domain limitation.
- 'ARP leaky VLAN' enables broadcasting of ARP packets to all other ports, ignoring the egress rule, when 'Broadcast leaky VLAN' is disabled.
- 'Multicast leaky VLAN' enables inter-VLAN multicast packet forwarding. Packets may be flooded to all the multicast address group member sets, ignoring the VLAN member set domain limitation.
- 'Inter-VLAN mirror function' enables the inter-VLAN mirror function, ignoring the VLAN member set domain limitation. The default value is 'Enable the inter-VLAN mirror'.

6.8. IEEE 802.1p Remarking Function

The RTL8309N provides IEEE 802.1p Remarking ability. Each port can enable or disable IEEE 802.1p Remarking ability. In addition, there is a RTL8309N global IEEE 802.1p Remarking Table. When one port enables 802.1p Remarking ability, 2-bit priority (not QID) determined by the RTL8309N is mapped to 3-bit priority according to the 1p Remarking Table.

If the port's 1p remarking function is enabled, transmitting VLAN tagged packets will have the 1Q VLAN tag's Priority field replaced with the 3-bit 1p remarking Priority.

When the VLAN tags are inserted to non-tagged packets, the inserted tag's priority will accord with the 1p remarking table, even if the port's 1p remarking function is disabled. When the VLAN tag is replaced on tagged packets and the 1p remarking function is disabled, the VLAN tag's VID will be replaced but the priority will not change. For a VLAN-tagged packet, the VID and 3-bit priority can be replaced by the RTL8309N independently.

6.9. Bandwidth Control Function

6.9.1. Input Bandwidth Control

The RTL8309N has input bandwidth control per port. If the speed of received packets is faster than the bandwidth setting of this port, the switch will send a pause frame to the link partner or drop packets, according to its flow control setting. The bandwidth granularity is 64Kbps.

6.9.2. Output Bandwidth Control

The RTL8309N has output bandwidth control per port, and has output bandwidth control on queue2 and queue3 in WRR mode. The bandwidth granularity is 64Kbps.

6.10. Quality of Service (QoS) Function

The RTL8309N identifies the priority of packets based on seven types of QoS priority information:

- Port-based
- IEEE 802.1Q-based
- DSCP-based
- IP priority-based

6.10.1. Priority Arbitration

The RTL8309N has one priority arbitration weight tables to decide which type of priority should be accepted when multiple types of priority exist. Each port can be set to its own Priority arbitration weight.

6.10.2. Port-Based Priority Assignment

Port-based priority assignment specifies a 2-bit priority for each physical port. When a packet is received from a physical port, it is assigned the 2-bit priority of that physical port. The port-based priority can be enabled or disabled by the control register.

6.10.3. IEEE 802.1Q-Based Priority Assignment

In IEEE 802.1Q-based priority assignment, when a packet is VLAN-tagged or priority-tagged, the 2-bit priority is mapping from 3-bit priority of the tag. When a packet is untagged, the 802.1Q-based priority is assigned to the default Dot1Q port-based 2-bit priority information of a physical port. The Dot1Q port-based priority can be enable or disable. When the priority comes from a packet, the 1Q-based priority is acquired by mapping 3-bit tag priority to 2-bit priority though a RTL8309N Dot1Q-based Priority Mapping Table. The Dot1Q-based priority can be enabled or disabled by the control register.

6.10.4. DSCP-Based Priority Assignment

The RTL8309N has one tables to map 6-bit DSCP values to 2-bit internal priorities. The table has 64 entries. The DSCP-based priority assignment can be enabled or disabled by the control register.

6.10.5. IP Address-Based Priority

When IP-based priority is enabled, any incoming packets with source or destination IP address equal to the configuration in register IP Priority Address [A] and IP Priority Mask [A], or IP Priority Address [B] and IP Priority Mask [B] will be set to a 2-bit priority.

IP priority [A] and IP priority [B] may be enabled or disabled independently. IP address-based priority can be enabled or disabled by the control register.

6.10.6. Internal Priority to Queue ID Table

The RTL8309N can transfer its internal priority to the output queue ID. Each port has a table with 4 entries to map the 2-bit internal priority to 2-bit queue ID.

6.10.7. Weighted Round-Robin

The RTL8309N has four queues per port. The Packet Scheduler controls the multiple traffic classes (i.e., controls the packet sending sequence of the priority queue). The RTL8309N supports Weighted Round-Robin (WRR) and Strict Priority (SP). Note that the Strict Priority queue is the highest priority of all queues, and overrides WRR. A larger strict priority queue ID indicates the priority is higher.

6.11. Layer2 Traffic Suppression Function (Storm Control)

The RTL8309N supports the storm filter function for each port. The storm types are broadcast storm, unknown only or all multicast storm, and unknown DA unicast storm. The RTL8309N can control all three storm types via three leaky buckets per port.

6.12. Input & Output Drop Function

If some destination ports are blocking or the buffer is full, the frames to these ports will be dropped.

There are two types of drop:

- Input Drop: Drop the frame directly. Do not forward to any port.
- Output Drop: Forward only to non-blocking ports.

For the RTL8309N, the dropping of broadcast, multicast, and unknown DA frames can be controlled independently.

6.13. Loop Detection Function

The RTL8309N periodically transmits a Realtek protocol frame to detect network loop faults. If a port detects a loop, the LED corresponding to the looped port will blink until the loop is resolved. At the same time, the loop event flag will be set.

6.14. Realtek Cable Tester Function

The RTL8309N features the Realtek Cable Tester (RTCT). The Cable Tester function can be used to detect a short (two conductors of pair short-circuited) or open (a lack of continuity between the pins at each end of the Ethernet cable, or a disconnected cable) in each differential pair, and report the result in corresponding registers. RTL8309N also has an LED per port to indicate test status and results.

6.15. EEPROM Configuration Function

RTL8309N can be initialed by EEPROM. To flexible initialize the register, RTL8309N used dynamic format to be loaded into any register needed to be initialized.

7. Interface Descriptions

7.1. I²C Master for EEPROM Auto-Download

Upon reset, the RTL8309N can auto-download the initial values of the internal MAC and PHY registers from the external EEPROM. The RTL8309N supports one types of EEPROM: 1Kb~16Kb.

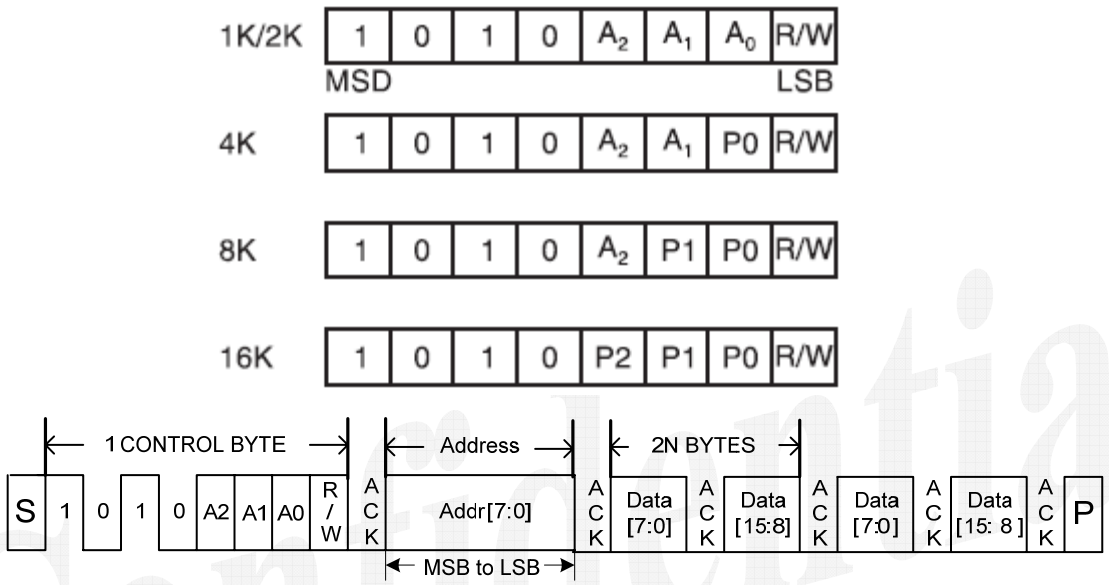


Figure 7. 1Kb~16Kb EEPROM Read/Write Timing

After a reset, the I2C module starts to access the external EEPROM as a master. The EEPROM auto-loading time varies with the size of the EEPROM. After the EEPROM auto-download, the I2C module will change to MDC/MDIO slave mode for external CPU access.

7.2. SMI Interface for External CPU Access

The RTL8309N supports a serial CPU interface (MDC/MDIO Slave mode) to access the internal registers (including all MAC and PHY configuration registers). There are two I/O pins (MDC and MDIO) for the SMI interface. MDIO is the access data signal, and MDC is the clock signal which frequency must be smaller than 3Mhz. The read/write data sequence is shown in Table 8-1.

Table 11. SMI (MDC, MDIO) Management Packet Format

Management Frame Fields

	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

8. LDO Regulator

RTL8309N embedded a LDO regulator from 3.3V to 1.0V that requires a well-designed PCB layout in order to achieve good power efficiency and lower the output voltage ripple and input overshoot. The LDO regulator 1.0V output pin must be connected only to DVDDL/AVDDL/AVDDLPLL (do not provide this power source to other devices).

Note: Refer to the separate RTL8309N layout guide for details.

9. Electrical Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 12. Absolute Maximum Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+125	°C
DVDDH, AVDDH, AVDDHPLL Supply Referenced to DGND, AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, AVDDLPLL Supply Referenced to DGND, AGND	GND-0.3	+1.20	V

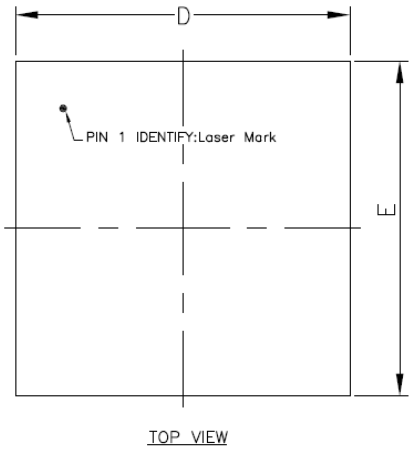
9.2. Recommended Operating Range

Table 13. Recommended Operating Range

Parameter	Min	Typical	Max	Units
DVDDH, AVDDH, AVDDHPLL Supply Voltage Range	3.135	3.3	3.465	V
DVDDL, AVDDL, AVDDLPLL Supply Voltage Range	0.95	1.0	1.05	V
Ambient Operating Temperature (Ta)	0	-	70	°C
Maximum Junction Temperature	-	-	125	°C

10. Mechanical Dimensions

10.1. Plastic Quad Flat No-Lead Package 64 Leads 9x9mm^2 Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E		9.00B SC			0.354 BSC	
D2/E2	5.75	6.00	6.25	0.226	0.236	0.246
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

11. Ordering Information

Table 14. Ordering Information

Part Number	Package	Status
	QFN 64-Pin E-PAD ‘Green’ Package	

Realtek Semiconductor Corp.
Headquarters
1F, No. 2, Industry East Road IX, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com.tw