Application Note:AN_ SY7203

30V High Current Boost LED Driver

Target Design Specification

General Description

SY7203 develops a step-up DC/DC converter that delivers an accurate constant current for driving LEDs. Operating at a fixed switching frequency of 1MHz allows the device to be used with small value external ceramic capacitors and inductor. The LED current is programmable through the external resistor. The device also supports PWM dimming for accurate LED current control.

SY7203 is ideal for driving up to eight white LEDs in series or up to 30V.

Features

- Input voltage range: 2.8 to 30V
- Switch current limit: 4A
- Drives LED strings up to 30V
- 1MHz fixed frequency minimizes the external components
- 20kHz~1MHz wide dimming frequency range for EN/PWM pin
- Internal softstart limits the inrush current
- Open LED over voltage protection
- RoHS Compliant and Halogen Free
- Compact package: DFN3X3-10

Ordering Information

SY7203 □(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY7203DBC	DFN3X3-10	

Applications

- GPS Navigation Systems
- Handheld Devices
- Portable Media Players

Typical Applications

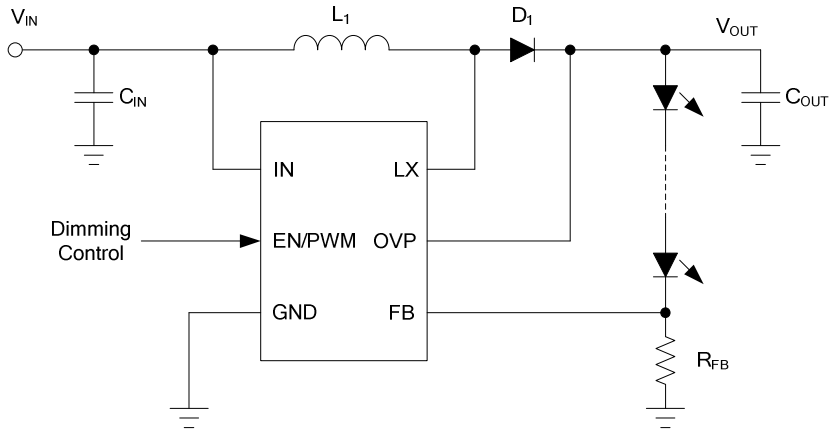
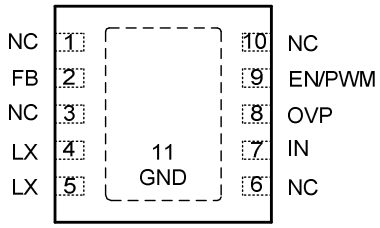


Figure 1. Schematic Diagram

Pinout (top view)



(DFN3X3-10)

Top mark：**NZ*xyz*** (Device code: NZ, ***x=year code, y=week code, z= lot number code***)

Pin Name	DFN3X3-10	Pin Description
LX	4, 5	Inductor node. Connect an inductor from power input to LX pin.
GND	Exposed Paddle	Ground pin
FB	2	Feedback pin. Connect a resistor R_{FB} between FB and GND to program the output current: ILED=0.2V/R_{FB}.
EN/PWM	9	Enable and dimming control. Pull high to turn on IC. The recommend dimming frequency range is 20kHz~1MHz.
OVP	8	Over voltage protection input. Connect to the output of circuit. The typical OVP value is 30V.
IN	7	Input pin. Decouple this pin to GND pin with 1uF ceramic cap.
NC	1, 3, 6, 10	No connection

Absolute Maximum Ratings

IN, EN/PWM ---------- 32V
LX, OVP ---------- 36V
All other pins ---------- 4V
Power Dissipation, PD @ TA = 25°C, DFN3X3-10 ----- ----------2.6 W
Package Thermal Resistance (Note 2)
DFN3X3-10, θ_{JA} ----------38°C/W
DFN3X3-10, θ_{JC} ----------8°C/W
Junction Temperature Range ---------- 125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions

Input Voltage Supply ---------- 2.8V to 30V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

(V_{IN} = 3.6V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2.8		30	V
Quiescent Current	I_Q	V_{FB}=0.3V		100	200	μA
Shutdown Current	I_{SHDN}	EN=0		10	15	μA
Feedback Reference Voltage	V_{REF}		196	200	204	mV
FB Input Current	I_{FB}	V_{FB}=0.3V			1	μA
Low Side Main FET RON	$R_{DS(ON)1}$			100		mΩ
Main FET Current Limit	I_{LIM1}		4			A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
IN UVLO Rising Threshold	$V_{IN,UVLO}$				2.4	V
UVLO Hysteresis	$U_{VLO,HYS}$			0.2		V
Switching Frequency	F_{SW}		0.8	1	1.2	MHz
Minimum ON Time	$T_{ON,MIN}$			100		nS
Maximum Duty Cycle	D_{MAX}			90		%
OVP Threshold	V_{OVP}	Open LED		30		V
Thermal Shutdown Temperature	T_{SD}			150		°C
Thermal Hysteresis	T_{HYS}			20		°C

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

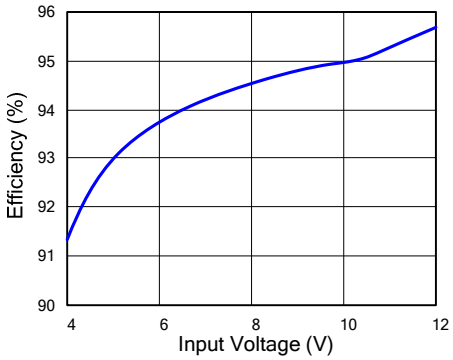
Note 2: Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions.

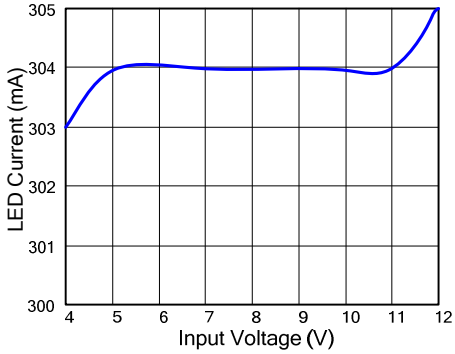
Typical Performance Characteristics

(V_{IN}=5V, I_{LED}=0.3A, 5PCS LED Series)

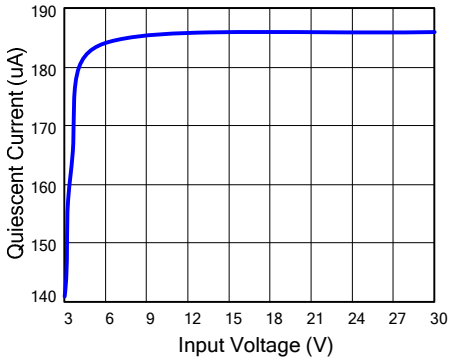
Efficiency vs. Input Voltage



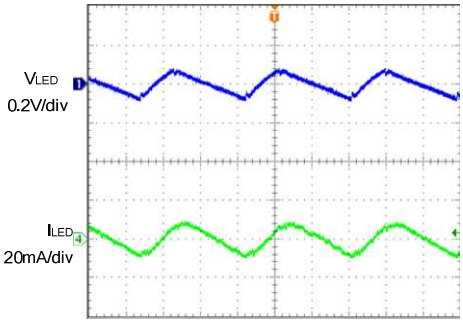
LED Current vs. Input Voltage



Quiescent Current vs. Input Voltage

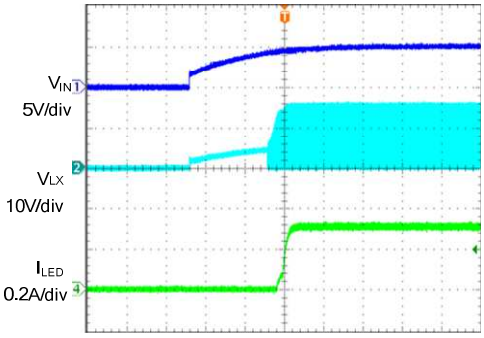


LED Current Pripple



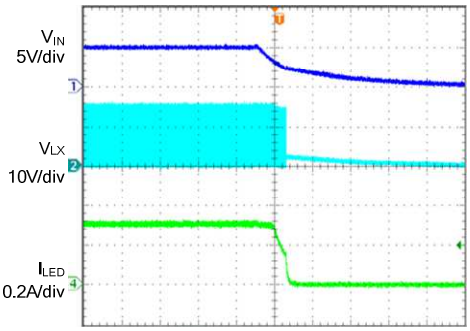
Time (400ns/div)

Startup from VIN



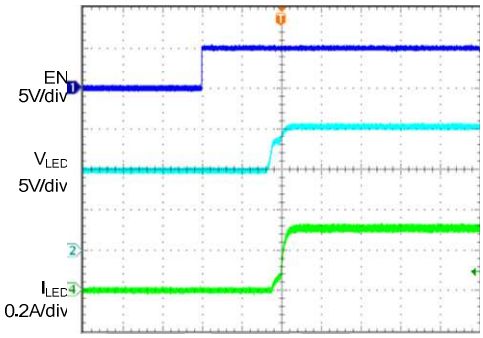
Time (2ms/div)

Shutdown from VIN



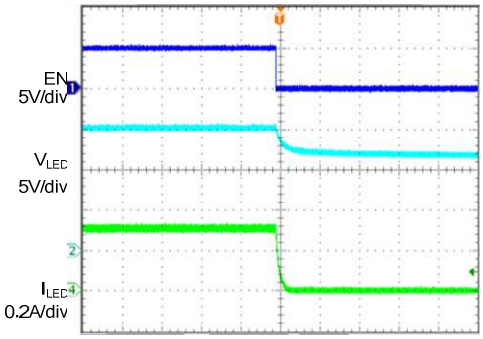
Time (400us/div)

Starup from Enable



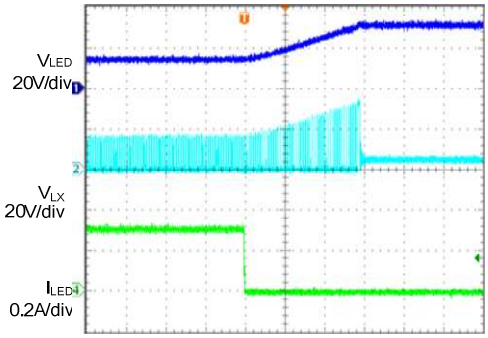
Time (2ms/div)

Shutdown from Enable



Time (2ms/div)

"Open LED"Protection



Time (20us/div)

Applications Information

Because of the high integration in the IC, the is simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, Schottky diode D and sense resistors R1 need to be selected for the targeted applications specifications.

Sense resistor R1 :

Choose R1 to program the proper LED Current. The R1 can be calculated to be:

$$R1 = \frac{0.2}{I_{LED}}$$

I_{LED} is the average LED current.

Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}}$$

An X5R or better grade ceramic capacitor with capacitance larger than 4.7uF is recommended to handle this ripple current. Place this ceramic capacitor really close to the IN and GND pins to minimize the potential noise problem. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{OUT,\,MAX} \cdot (V_{OUT} - V_{IN})}{F_{SW} \cdot V_{OUT} \cdot V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple.

For LED applications, the equivalent resistance of the LED is typically low. The output capacitance should be large enough to attenuate the ripple current through LED. A capacitor larger than 2.2uF is recommended.

Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT,\,MAX} \times 40\%}$$

where F_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY7203 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,\,MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT,\,MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mohm to achieve a good overall efficiency.

Schottky Diode D:

Because of high switching speed of SY7203/SY7203A, a Schottky diode with low forward voltage drop and fast switching speed is desirable for the application. The voltage rating of the diode must be higher than maximum output voltage. The diode's average and peak current rating should exceed the average output current and peak inductor current.

Dimming Control

SY7203 and SY7203A offer several different dimming schemes for LED brightness control. One way is to apply a PWM signal to the EN/PWM pin. Fig.2 shows the internal block diagram of the dimming circuit of SY7203. The PWM signal changes the regulation

voltage by change the duty cycle. The relationship between the duty cycle and FB voltage is calculated as: V_{FB}=Duty*200mV

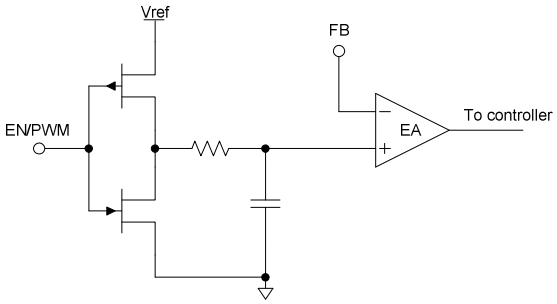


Figure 2

Since the cut-off frequency of the internal low pass filter is near 5kHz, it is recommended selecting the PWM signal frequency to be higher than 20kHz.

SY7203A adopts direct PWM dimming control as shown in Fig.3. The EN/PWM directly controls the driver of power MOSFET. The internal MOSFET turns off when EN/PWM signal is low. And the MOSFET resumes switching when EN/PWM signal is high.

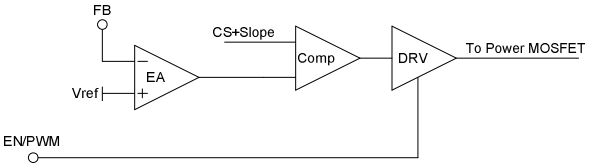


Figure 3

Another way is to use a DC voltage as shown in Fig.4. The LED current decreases as the DC voltage rises. The relationship between LED current and DC voltage is:

$$I_{LED} = \frac{V_{REF} \times (R_1 + R_2) - V_{DC} \times R_1}{R_2 \times R_{FB}}$$

Where V_{REF} is the 200mV internal reference voltage, VDC is the dimming DC voltage.

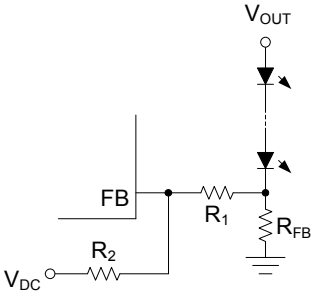


Figure 4

A filtered PWM signal can be used to substituted the DC input as shown in Fig.5.To better filter out the AC components of the PWM signal, it is recommend choosing the same value for R2 and R3 and the cut-off frequency of the low pass filter (formed by R2//R3 and C1) to be well below the dimming signal frequency. The LED current decreases as the duty cycle increases. The LED current can be calculated using equation below:

$$I_{LED} = \frac{V_{REF} \times (R_1 + R_2 + R_3) - V_{PWM} \times Duty \times R_1}{(R_2 + R_3) \times R_{FB}}$$

Where V_{REF} is the 200mV internal reference voltage, V_{PWM} is the high voltage level of PWM signal, Duty is the duty cycle of PWM signal.

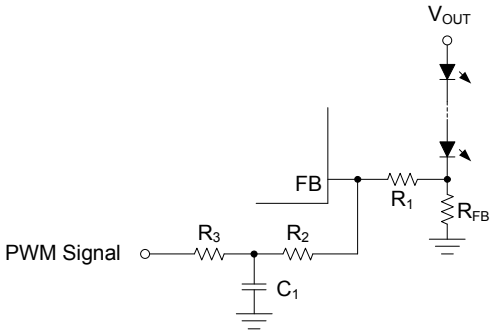


Figure 5

Layout Design:

The layout design of SY7203/SY7203A regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{IN}, C_{OUT}, L, R1 and D.

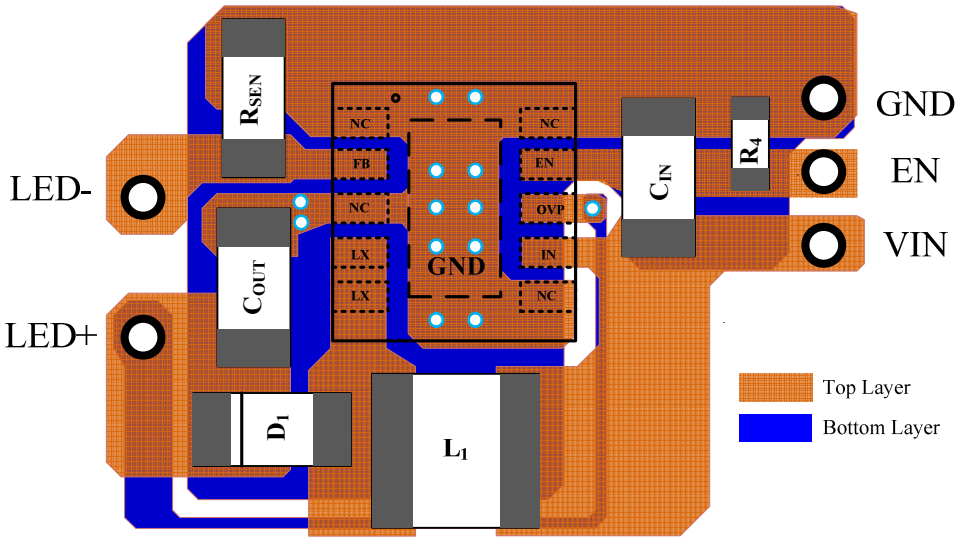
1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

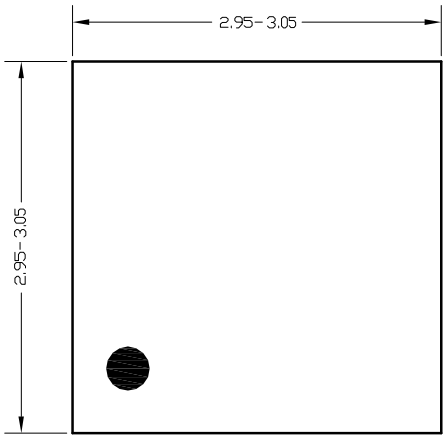
3) Minimize the loop area of LX, D, C_{OUT} and GND.
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

5) The components R1, the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

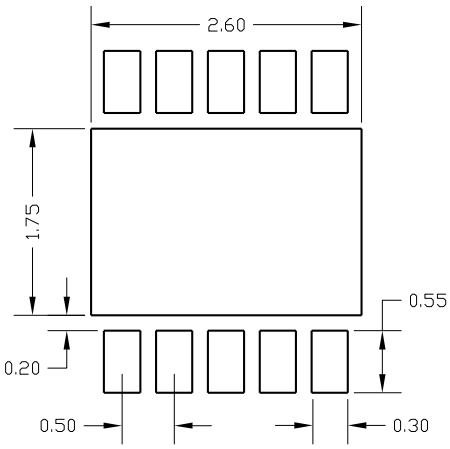
6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.



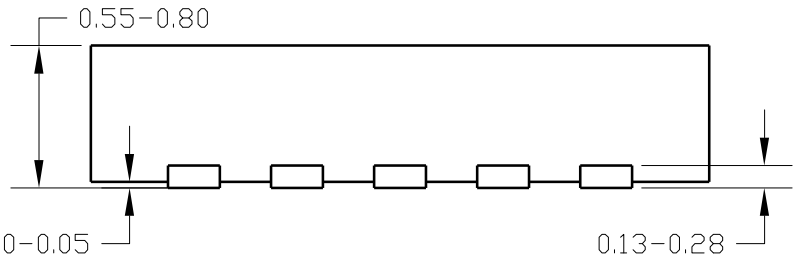
DFN3x3-10 Package outline



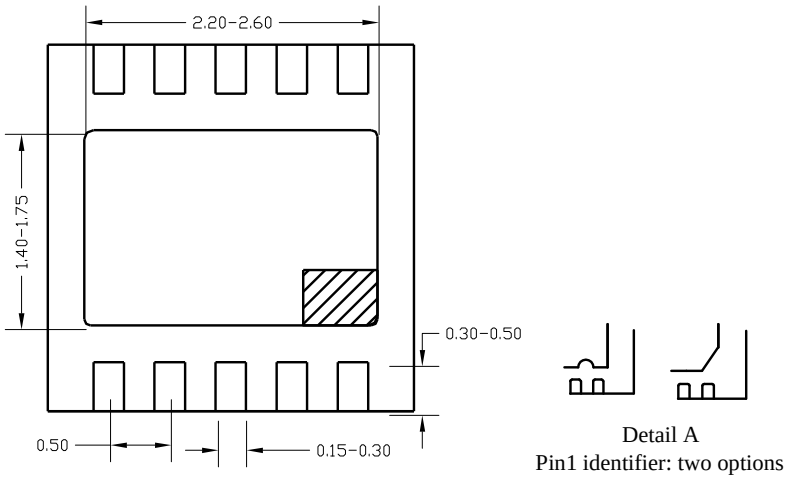
Top View



PCB layout (recommended)



Side View



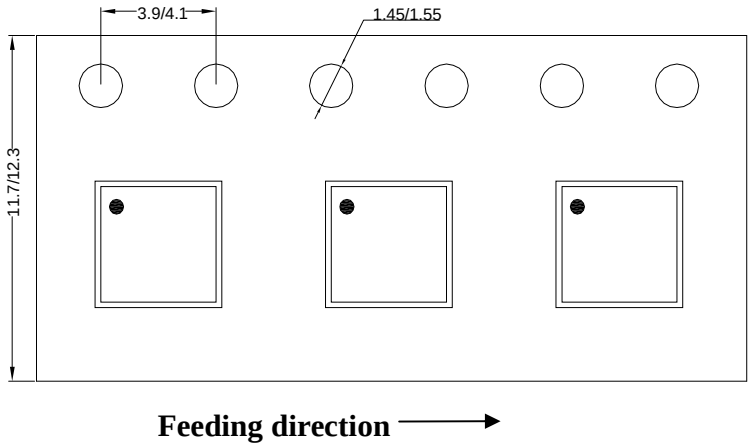
Detail A
Pin1 identifier: two options

Bottom View

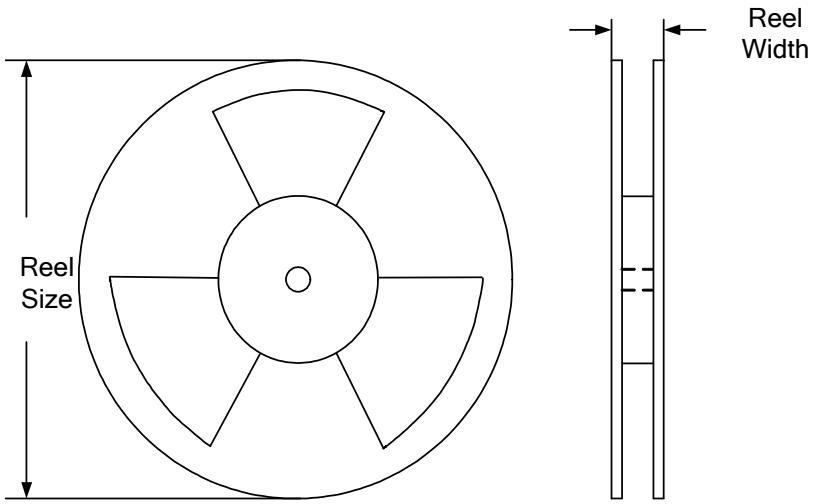
Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

Taping & Reel Specification

1. DFN3x3-10 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3-10	10	8	13"	12.4	400	400	5000

3. Others: NA