TL331 Single Differential Comparator

1 Features

- Single Supply or Dual Supplies
- Wide Range of Supply Voltage, 2 V to 36 V
- Low Supply-Current Drain Independent of Supply Voltage, 0.4 mA Typ
- Low Input Bias Current, 25 nA Typ
- Low Input Offset Voltage, 2 mV Typ
- Common-Mode Input Voltage Range Includes Ground
- Differential Input Voltage Range Equal to Maximum-Rated Supply Voltage, ±36 V
- Low Output Saturation Voltage
- Output Compatible With TTL, MOS, and CMOS

2 Applications

- Hysteresis Comparators
- Oscillators
- Window Comparators
- Industrial Equipment
- Test and Measurement

3 Description

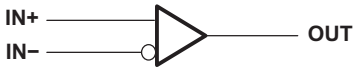
This device consists of a single voltage comparator that is designed to operate from a single power supply over a wide range of voltages. Operation from dual supplies also is possible if the difference between the two supplies is 2 V to 36 V and V_{CC} is at least 1.5 V more positive than the input common-mode voltage. Current drain is independent of the supply voltage. The output can be connected to other open-collector outputs to achieve wired-AND relationships.

Device Information(1)

PART NUMBER	PACKAGE (PIN)	BODY SIZE (NOM)
TL331	SOT (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematic



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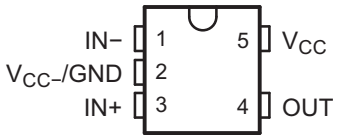
5 Revision History

Changes from Revision F (July 2008) to Revision G **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Deleted *Ordering Information* table. ... 1
- Deleted 25°C Specifications in *Electrical Characteristics* table. ... 5
- Changed test condition V_{ID} for parameter I_{OL} from 1 V to –1 V in *Electrical Characteristics* table. ... 5

6 Pin Configuration and Functions

DBV PACKAGE
(TOP VIEW)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
IN+	3	I	Positive Input
IN–	1	I	Negative Input
OUT	4	O	Open Collector/Drain Output
V_{CC}	5	I	Power Supply Input
GND	2	I	Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	0	36	V
V_{ID}	Differential input voltage(3)	–36	36	V
V_I	Input voltage range (either input)	–0.3	36	V
V_O	Output voltage	0	36	V
I_O	Output current	0	20	mA
	Duration of output short-circuit to ground(4)	Unlimited		
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the network ground.
(3) Differential voltages are at IN+ with respect to IN–.
(4) Short circuits from outputs to V_{CC} can cause excessive heating and eventual destruction.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2	36	V
T_J	Junction Temperature	-40	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TL331 DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	218.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	87.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	44.9	
ψ_{JT}	Junction-to-top characterization parameter	4.3	
ψ_{JB}	Junction-to-board characterization parameter	44.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

at specified free-air temperature, V_{CC} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)	T_A (2)	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_{CC} = 5 V to 30 V, V_O = 1.4 V, $V_{IC} = V_{IC(min)}$	25°C		2	5	mV
			Full range			9	
I_{IO}	Input offset current	V_O = 1.4 V	25°C		5	50	nA
			Full range			250	
I_{IB}	Input bias current	V_O = 1.4 V	25°C		–25	–250	nA
			Full range			–400	
V_{ICR}	Common-mode input voltage range(3)		Full range	0 to V_{CC} – 1.5			V
A_{VD}	Large-signal differential voltage amplification	V_{CC} = 15 V, V_O = 1.4 V to 11.4 V, $R_L \geq 15$ kΩ to V_{CC}	25°C	50	200		V/mV
I_{OH}	High-level output current	V_{OH} = 5 V, V_{ID} = 1 V	25°C		0.1	50	nA
		V_{OH} = 30 V, V_{ID} = 1 V	Full range			1	µA
V_{OL}	Low-level output voltage	I_{OL} = 4 mA, V_{ID} = –1 V	25°C		150	400	mV
			Full range			700	
I_{OL}	Low-level output current	V_{OL} = 1.5 V, V_{ID} = –1 V	25°C	6			mA
I_{CC}	Supply current	$R_L = \infty$, V_{CC} = 5 V	25°C		0.4	0.7	mA

(1) All characteristics are measured with zero common-mode input voltage, unless otherwise specified.
(2) Full range T_A is –40°C to 85°C for I-suffix devices and –40°C to 105°C for K-suffix devices.
(3) The voltage at either input or common-mode should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either or both inputs can go to 30 V without damage.

7.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TYP	UNIT
Response time	R_L connected to 5 V through 5.1 kΩ, C_L = 15 pF(1) (2)	100-mV input step with 5-mV overdrive	1.3	µs
		TTL-level input step	0.3	

(1) C_L includes probe and jig capacitance.
(2) The response time specified is the interval between the input step function and the instant when the output crosses 1.4 V.

7.7 Typical Characteristics

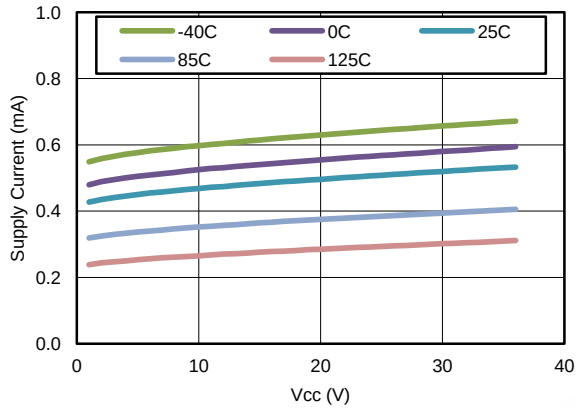


Figure 1. Supply Current vs Supply Voltage

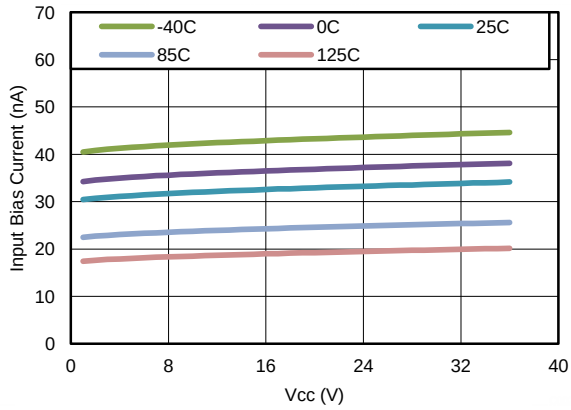


Figure 2. Input Bias Current vs Supply Voltage

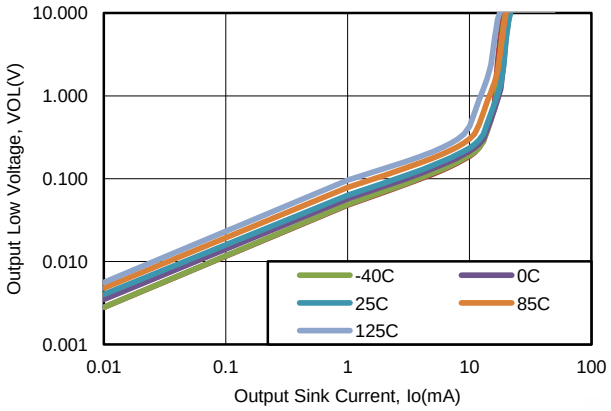


Figure 3. Output Low Voltage vs Output Current (I_{OL})

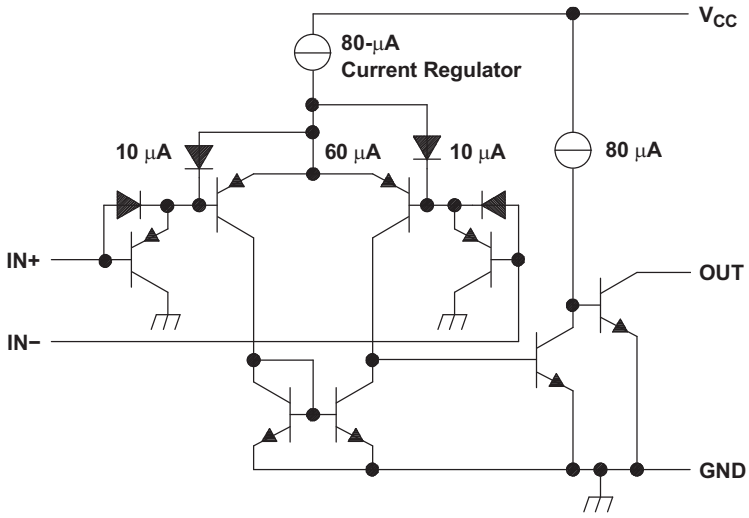
8 Detailed Description

8.1 Overview

The TL331 is a single comparator with the ability to operate up to 36 V on the supply pin. This standard device has proven ubiquity and versatility across a wide range of applications. This is due to it's very wide supply voltages range (2 V to 36 V), low Iq and fast response.

The open-drain output allows the user to configure the output's logic low voltage (V_{OL}) and can be utilized to enable the comparator to be used in AND functionality.

8.2 Functional Block Diagram



COMPONENT COUNT	
Epi-FET	1
Diodes	2
Resistors	1
Transistors	20

Current values shown are nominal.

8.3 Feature Description

TL331 consists of a PNP darlington pair input, allowing the device to operate with very high gain and fast response with minimal input bias current. The input Darlington pair creates a limit on the input common mode voltage capability, allowing TL331 to accurately function from ground to V_{CC} – 1.5 V differential input. This is enables much head room for modern day supplies of 3.3 V and 5.0 V.

The output consists of an open drain NPN (pull-down or low side) transistor. The output NPN will sink current when the positive input voltage is higher than the negative input voltage and the offset voltage. The VOL is resistive and will scale with the output current. Please see Figure 3 for V_{OL} values with respect to the output current.

8.4 Device Functional Modes

8.4.1 Voltage Comparison

The TL331 operates solely as a voltage comparator, comparing the differential voltage between the positive and negative pins and outputting a logic low or high impedance (logic high with pull-up) based on the input differential polarity.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

TL331 will typically be used to compare a single signal to a reference or two signals against each other. Many users take advantage of the open drain output to drive the comparison logic output to a logic voltage level to an MCU or logic device. The wide supply range and high voltage capability makes TL331 optimal for level shifting to a higher or lower voltage.

9.2 Typical Application

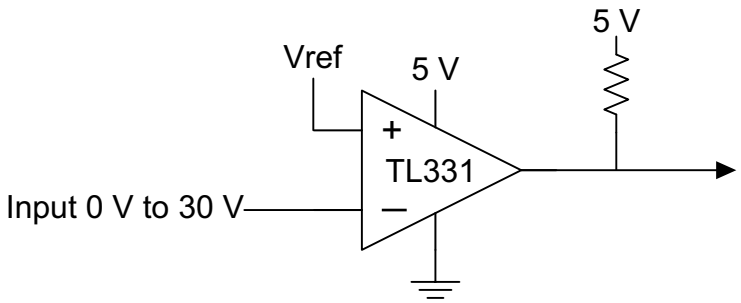


Figure 4. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	0 V to V_{CC} – 1.5 V
Supply Voltage	2 V to 36 V
Logic Supply Voltage (R_{PULLUP} Voltage)	2 V to 36 V
Output Current (V_{LOGIC}/R_{PULLUP})	1 µA to 20 mA
Input Overdrive Voltage	100 mV
Reference Voltage	2.5 V
Load Capacitance (C_L)	15 pF

9.2.2 Detailed Design Procedure

When using TL331 in a general comparator application, determine the following:

- Input voltage range
- Minimum overdrive voltage
- Output and drive current
- Response time

9.2.2.1 Input Voltage Range

When choosing the input voltage range, the input common mode voltage range (V_{ICR}) must be taken in to account. If temperature operation is above or below 25°C the V_{ICR} can range from 0 V to V_{CC} – 1.5 V. This limits the input voltage range to as high as V_{CC} – 1.5 V and as low as 0 V. Operation outside of this range can yield incorrect comparisons.

Below is a list of input voltage situation and their outcomes:

1. When both IN- and IN+ are both within the common mode range:
   (a) If IN- is higher than IN+ and the offset voltage, the output is low and the output transistor is sinking current
   (b) If IN- is lower than IN+ and the offset voltage, the output is high impedance and the output transistor is not conducting
2. When IN- is higher than common mode and IN+ is within common mode, the output is low and the output transistor is sinking current
3. When IN+ is higher than common mode and IN- is within common mode, the output is high impedance and the output transistor is not conducting
4. When IN- and IN+ are both higher than common mode, the output is low and the output transistor is sinking current

9.2.2.2 Minimum Overdrive Voltage

Overdrive Voltage is the differential voltage produced between the positive and negative inputs of the comparator over the offset voltage (V_{IO}). In order to make an accurate comparison the Overdrive Voltage (V_{OD}) should be higher than the input offset voltage (V_{IO}). Overdrive voltage can also determine the response time of the comparator, with the response time decreasing with increasing overdrive. Figure 5 and Figure 6 show positive and negative response times with respect to overdrive voltage.

9.2.2.3 Output and Drive Current

Output current is determined by the load/pull-up resistance and logic/pull-up voltage. The output current will produce a output low voltage (V_{OL}) from the comparator. In which V_{OL} is proportional to the output current. Use Figure 3 to determine V_{OL} based on the output current.

The output current can also effect the transient response. More will be explained in the next section.

9.2.2.4 Response Time

The transient response can be determined by the load capacitance (C_L), load/pull-up resistance (R_{PULLUP}) and equivalent collector-emitter resistance (R_{CE}).

- The positive response time (τ_p) is approximately $\tau_P \sim R_{PULLUP} \times C_L$
- The negative response time (τ_N) is approximately $\tau_N \sim R_{CE} \times C_L$
  – R_{CE} can be determine by taking the slope of Figure 3 in it's linear region at the desired temperature, or by dividing the V_{OL} by I_{out}

9.2.3 Application Curves

The following curves were generated with 5 V on V_{CC} and V_{Logic}, R_{PULLUP} = 5.1 kΩ, and 50 pF scope probe.

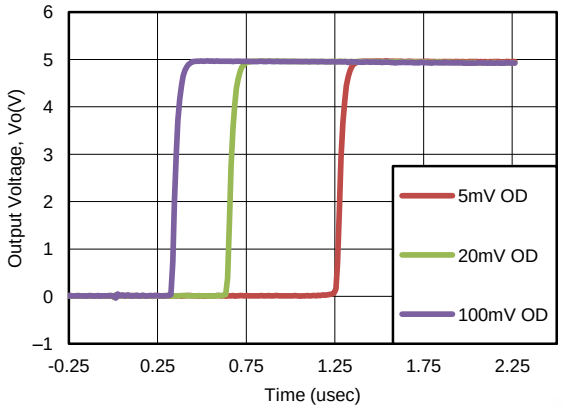


Figure 5. Response Time for Various Overdrives (Positive Transition)

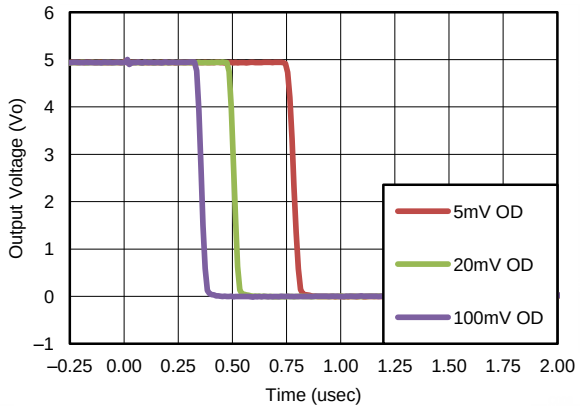


Figure 6. Response Time for Various Overdrives (Negative Transition)

10 Power Supply Recommendations

For fast response and comparison applications with noisy or AC inputs, it is recommended to use a bypass capacitor on the supply pin to reject any variation on the supply voltage. This variation can eat into the comparator's input common mode range and create an inaccurate comparison.

11 Layout

11.1 Layout Guidelines

For accurate comparator applications without hysteresis it is important maintain a stable power supply with minimized noise and glitches, which can affect the high level input common mode voltage range. In order to achieve this, it is best to add a bypass capacitor between the supply voltage and ground. This should be implemented on the positive power supply and negative supply (if available). If a negative supply is not being used, do not put a capacitor between the IC's GND pin and system ground.

11.2 Layout Example

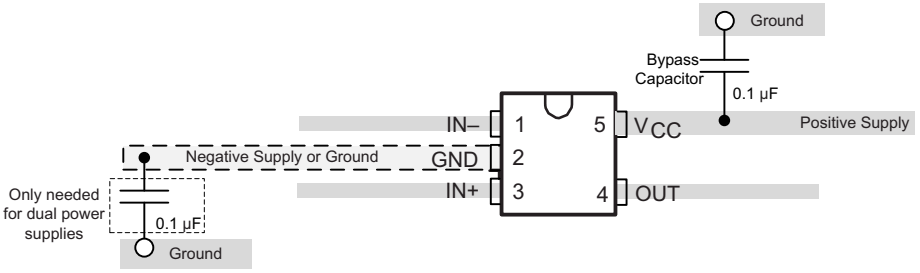


Figure 7. TL331 Layout Example

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL331IDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T1IG ~ T1IL ~ T1IS)	Samples
TL331IDBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1IG	Samples
TL331IDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1IG	Samples
TL331IDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	(T1IG ~ T1IL ~ T1IU)	Samples
TL331IDBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	T1IG	Samples
TL331KDBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1KG ~ T1KL)	Samples
TL331KDBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 105	(T1KG ~ T1KL)	Samples
TL331KDBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-40 to 105	(T1KG ~ T1KL)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TL331 :

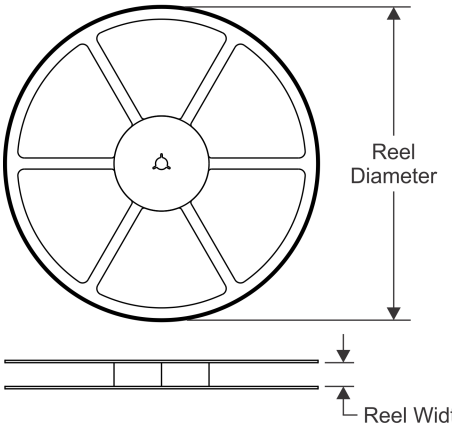
- Automotive: TL331-Q1
- Enhanced Product: TL331-EP

NOTE: Qualified Version Definitions:

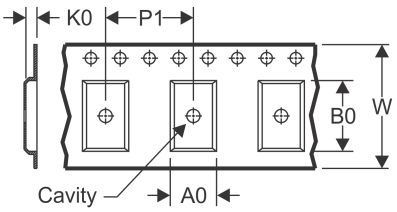
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

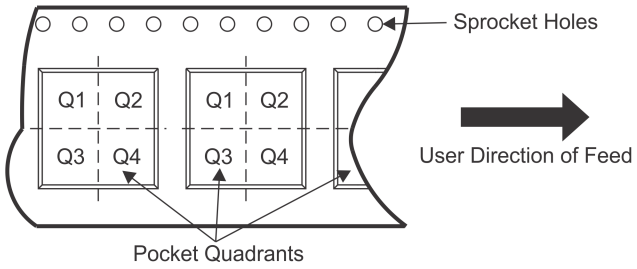


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

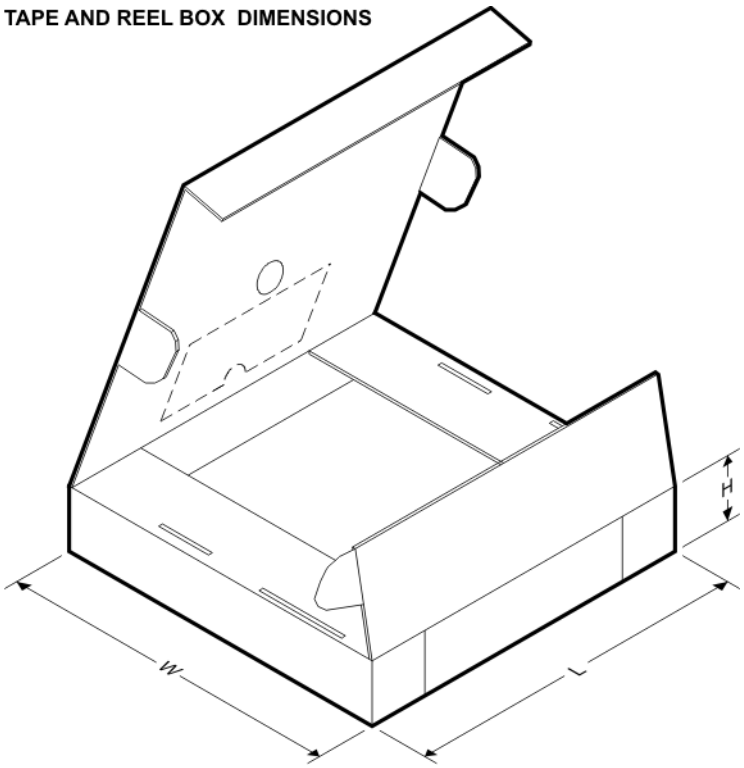
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL331IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL331IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TL331IDBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TL331IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TL331IDBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TL331KDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

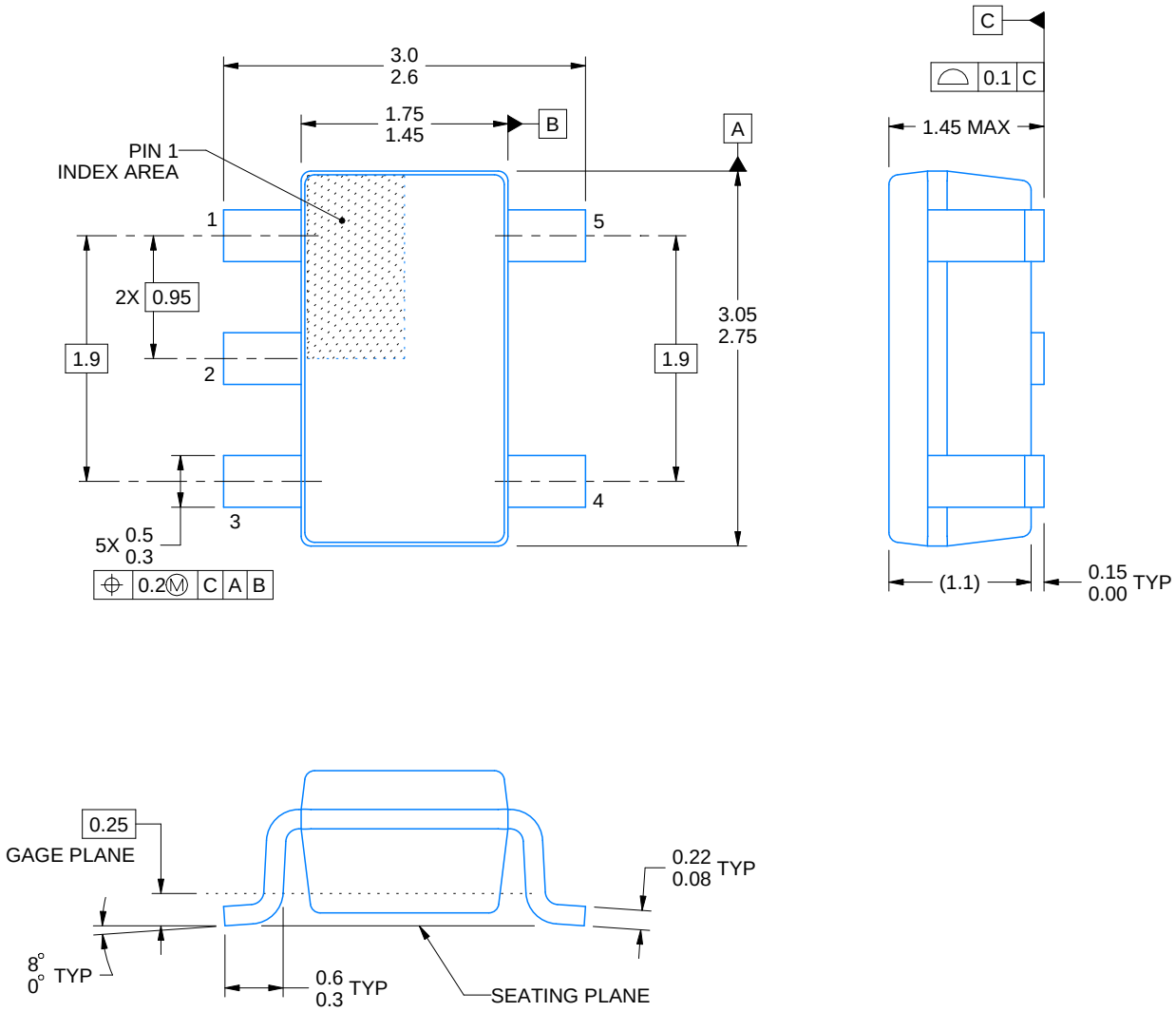
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL331IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL331IDBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
TL331IDBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TL331IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TL331IDBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
TL331KDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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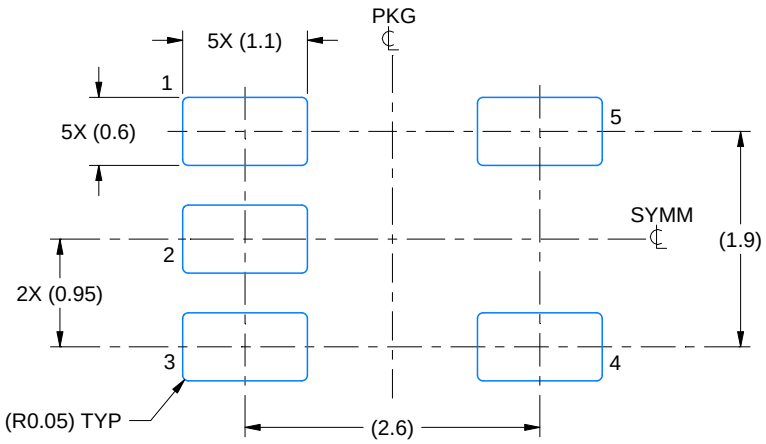
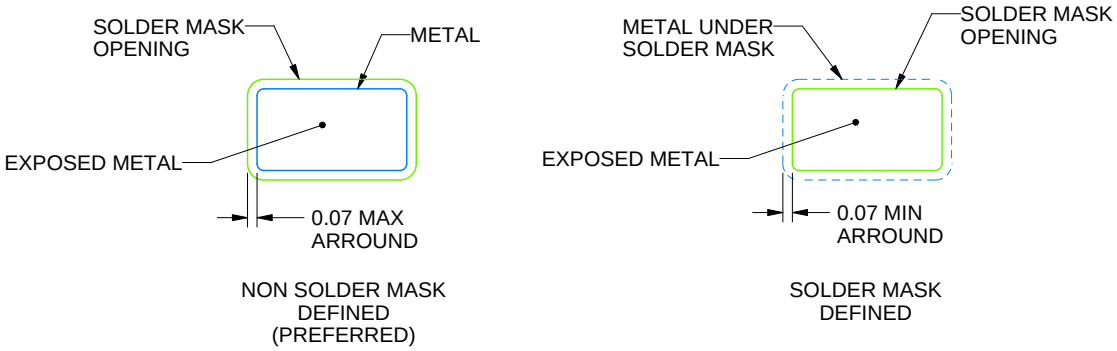
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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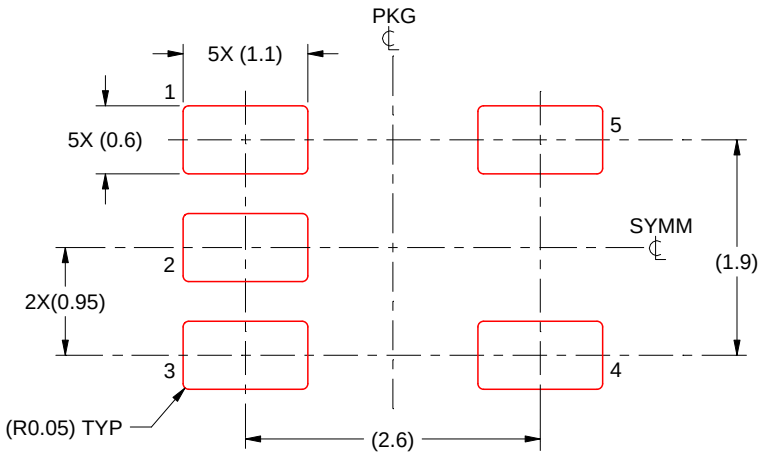
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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