HGSEMI

LM324

Low power quad operational amplifiers

Features

- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current per amplifier: 375 µA
- Low input bias current: 20 nA
- Low input offset voltage: 5 mV max.
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: +3 V to +30 V
- Dual supplies: ±1.5 V to ±15 V

N
DIP14
(Plastic package)

D
SO-14
(Plastic micropackage)

Description

These circuits consist of four independent, high gain, internally frequency-compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

1 Pin and schematic diagram

Figure 1. Pin connections (top view)

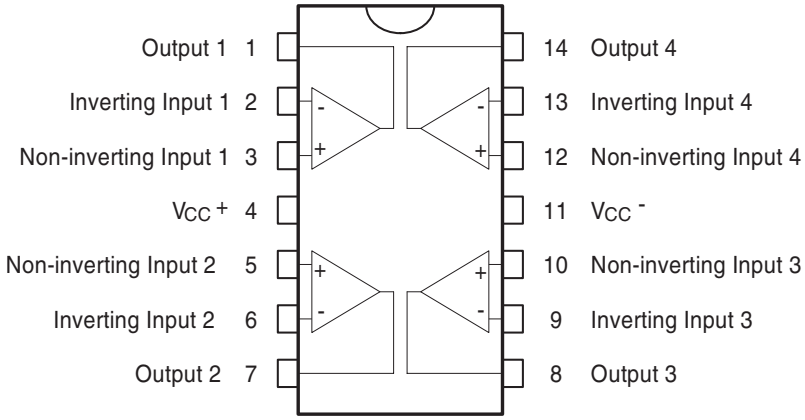
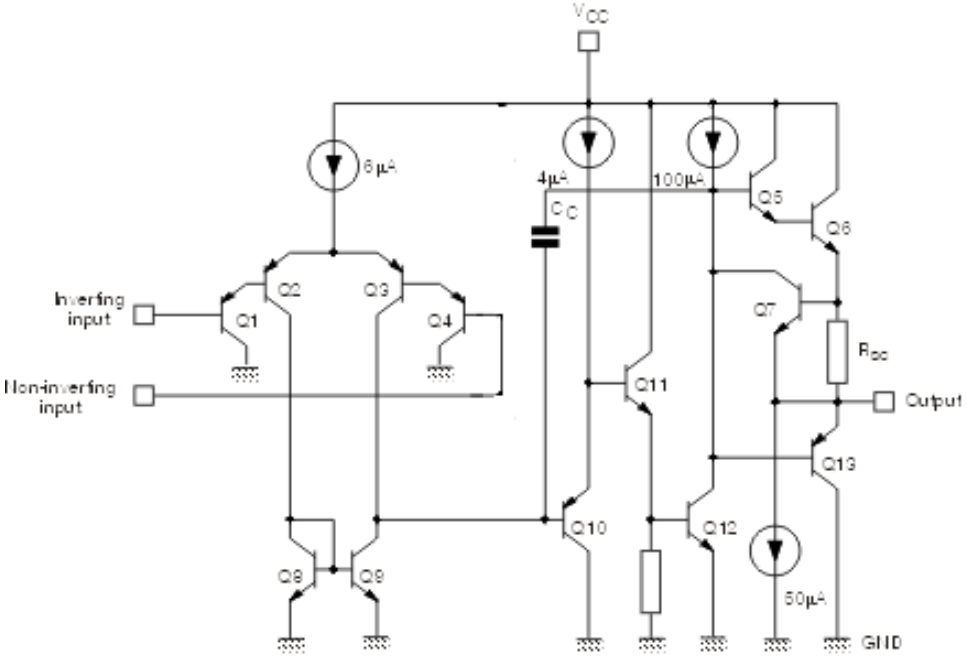


Figure 2. Schematic diagram (1/4 LM124)



2 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	LM324	Unit
V_{CC}	Supply voltage	±16 or 32	V
V_{in}	Input voltage(1)	-0.3 to 32	V
V_{id}	Differential input voltage (2)	32	V
	Output short-circuit duration (3)	Infinite	
I_{in}	Input current (4): V_{in} driven negative Input current (5): V_{in} driven positive above AMR value	5 mA in DC or 50 mA in AC (duty cycle = 10%, T=1s) 0.4	mA
T_{oper}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thja}	Thermal resistance junction to ambient(6) SO14 DIP14	 103 83	°C/W
R_{thjc}	Thermal resistance junction to case SO14 DIP14	 31 33	°C/W
ESD	HBM: human body model(7)	250	V
	MM: machine model(8)	150	
	CDM: charged device model(9)	1500	

1. Either or both input voltages must not exceed the magnitude of V_{CC}^+ or V_{CC}^-. All voltage values, except differential voltages are with respect to ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
3. Short-circuits from the output to V_{CC} can cause excessive heating if V_{CC} > 15 V. The maximum output current is approximately 40 mA independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
4. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
5. The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400 µA max (R = (Vin - 32 V)/400 µA).
6. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These are typical values given for a single layer board (except for TSSOP, a two-layer board).
7. Human body model, 100 pF discharged through a 1.5 kΩ resistor into pin of device.
8. Machine model ESD: a 200 pF capacitor is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5 Ω), into pin-to-pin of device.
9. Charged device model: all pins plus package are charged together to the specified voltage and then discharged directly to ground.

3 Electrical characteristics

Table 2. V_{CC}^+ = +5 V, V_{CC}^-= ground, V_o = 1.4 V, T_{amb} = +25° C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage (1) T_{amb} = +25° C LM324			7	mV
	$T_{min} \le T_{amb} \le T_{max}$ LM324			9	
I_{io}	Input offset current T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$		2	30 100	nA
I_{ib}	Input bias current (2) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$		20	150 300	nA
A_{vd}	Large signal voltage gain V_{CC}^+ = +15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	 50 25	 100		V/mV
SVR	Supply voltage rejection ratio ($R_s \le 10$ kΩ) V_{CC}^+ = 5 V to 30 V T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	 65 65	 110		dB
I_{CC}	Supply current, all Amp, no load T_{amb} = +25° C V_{CC} = +5 V V_{CC} = +30 V		 0.7 1.5	 1.2 3	mA
	$T_{min} \le T_{amb} \le T_{max}$ V_{CC} = +5 V V_{CC} = +30 V		 0.8 1.5	 1.2 3	
V_{icm}	Input common mode voltage range V_{CC} = +30 V (3) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	 0 0		 V_{CC} -1.5 V_{CC} -2	V
CMR	Common mode rejection ratio ($R_s \le 10$ kΩ) T_{amb} = +25° C $T_{min} \le T_{amb} \le T_{max}$	 70 60	 80		dB
I_{source}	Output current source (V_{id} = +1 V) V_{CC} = +15 V, V_o = +2 V	20	40	70	mA

Table 2. V_{CC}^+ = +5 V, V_{CC}^-= ground, V_o = 1.4 V, T_{amb} = +25° C (unless otherwise specified) (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{sink}	Output sink current (V_{id} = -1 V) V_{CC} = +15 V, V_o = +2 V V_{CC} = +15 V, V_o = +0.2 V	 10 12	 20 50		 mA µA
V_{OH}	High level output voltage V_{CC} = +30 V T_{amb} = +25° C, R_L = 2 kΩ $T_{min} \le T_{amb} \le T_{max}$ T_{amb} = +25° C, R_L = 10 kΩ $T_{min} \le T_{amb} \le T_{max}$	 26 26 27 27	 27 28		 V
	V_{CC} = +5 V, R_L = 2 kΩ T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$	 3.5 3			
V_{OL}	Low level output voltage (R_L = 10 kΩ) T_{amb} = +25°C $T_{min} \le T_{amb} \le T_{max}$		5	 20 20	mV
SR	Slew rate V_{CC} = 15 V, V_i = 0.5 to 3 V, R_L = 2 kΩ, C_L = 100 pF, unity gain		0.4		V/µs
GBP	Gain bandwidth product V_{CC} = 30 V, f = 100 kHz, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF		1.3		MHz
THD	Total harmonic distortion f = 1 kHz, A_v = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC} = 30 V		0.015		%
e_n	Equivalent input noise voltage f = 1 kHz, R_s = 100 Ω, V_{CC} = 30 V		40		$\frac{nV}{\sqrt{Hz}}$
DV_{io}	Input offset voltage drift		7	30	µV/°C
DI_{io}	Input offset current drift		10	200	pA/°C
V_{o1}/V_{o2}	Channel separation (4) 1 kHz ≤ f ≤ 20 kHZ		120		dB

1. V_o = 1.4 V, R_s = 0 Ω, 5 V < V_{CC}^+ < 30 V, 0 < V_{ic} < V_{CC}^+ - 1.5 V.
2. The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.
3. The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0. V. The upper end of the common-mode voltage range is V_{CC}^+ - 1.5 V, but either or both inputs can go to +32 V without damage.
4. Due to the proximity of the external components, ensure that stray capacitance between these external parts does not cause coupling. Coupling can be detected because this type of capacitance increases at higher frequencies.

Figure 3. Input bias current vs. ambient temperature

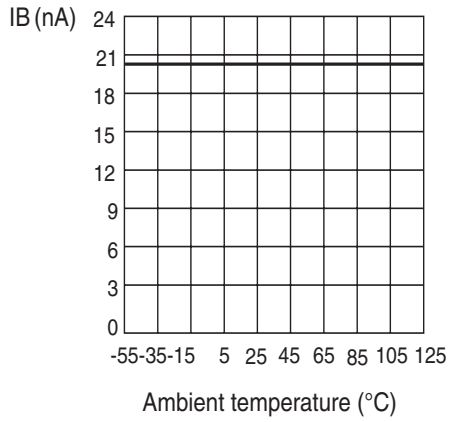


Figure 4. Current limiting

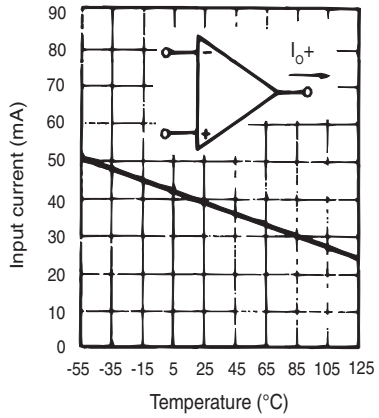


Figure 5. Input voltage range

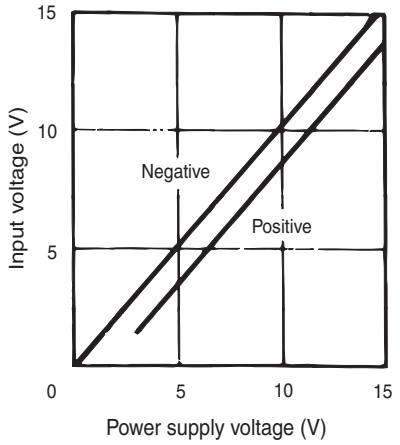


Figure 6. Supply current

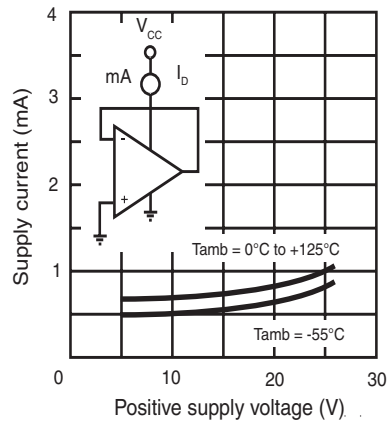


Figure 7. Gain bandwidth product

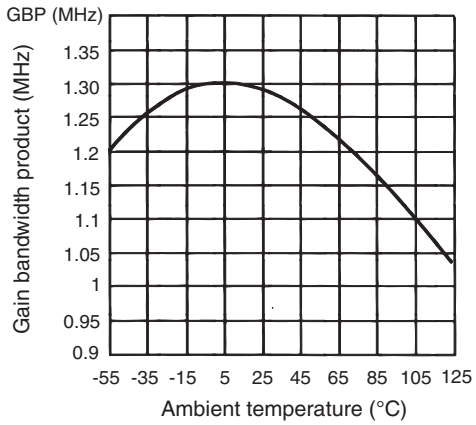


Figure 8. Common mode rejection ratio

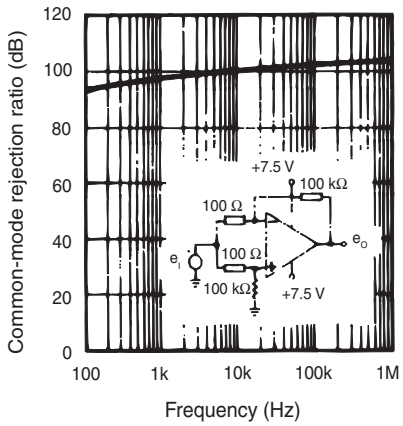


Figure 9. Open loop frequency response

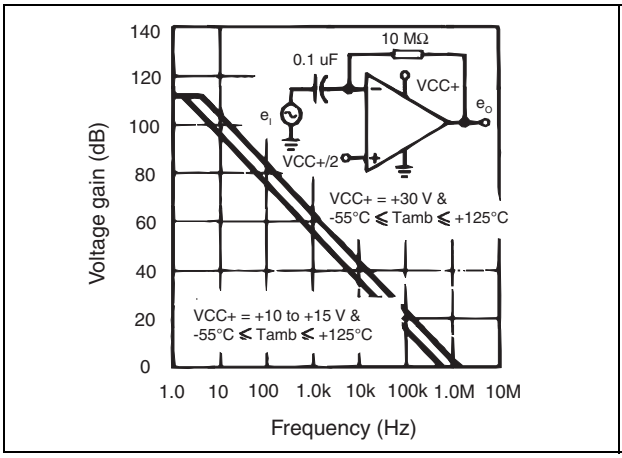


Figure 10. Large signal frequency response

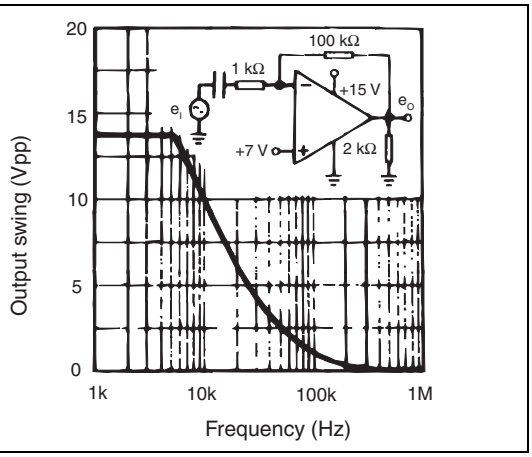


Figure 11. Voltage follower pulse response

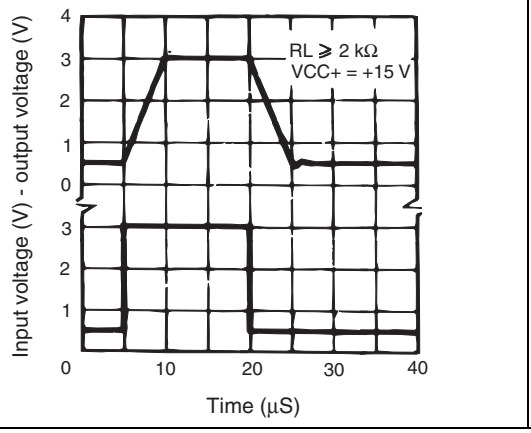


Figure 12. Output characteristics (current sinking)

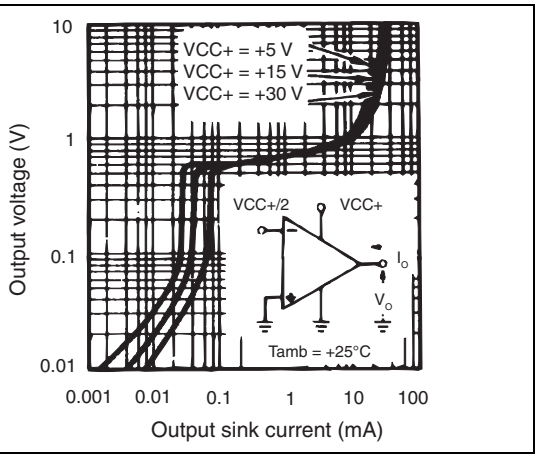


Figure 13. Voltage follower pulse response (small signal)

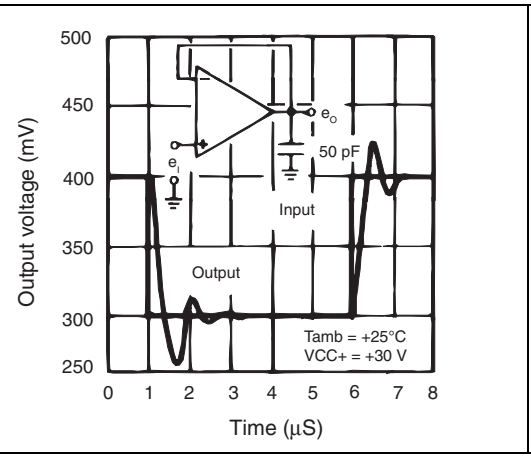


Figure 14. Output characteristics (current sourcing)

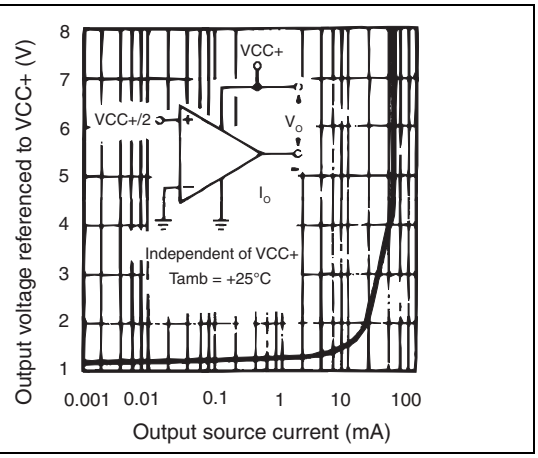


Figure 15. Input current

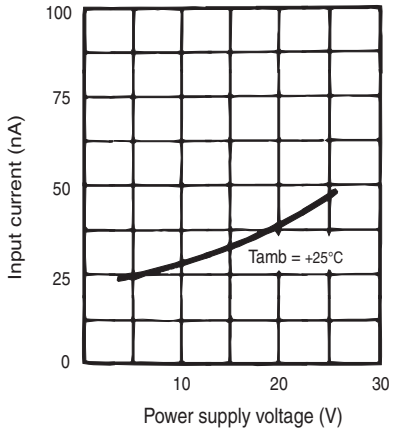


Figure 16. Large signal voltage gain

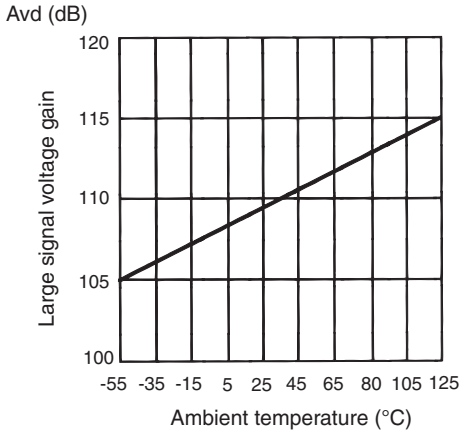


Figure 17. Power supply and common mode rejection ratio

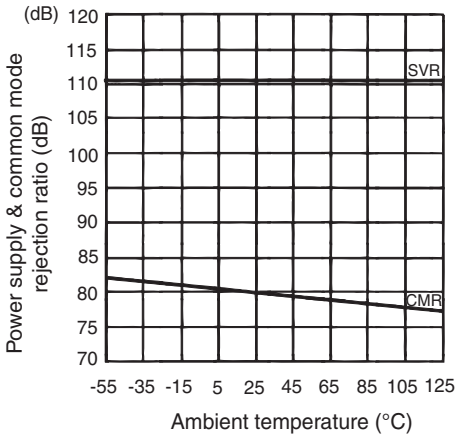
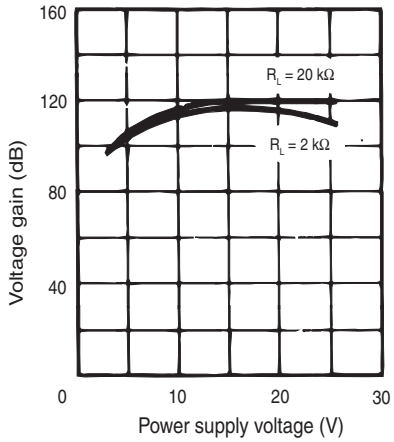


Figure 18. Voltage gain



4 Typical single-supply applications

Figure 19. AC coupled inverting amplifier

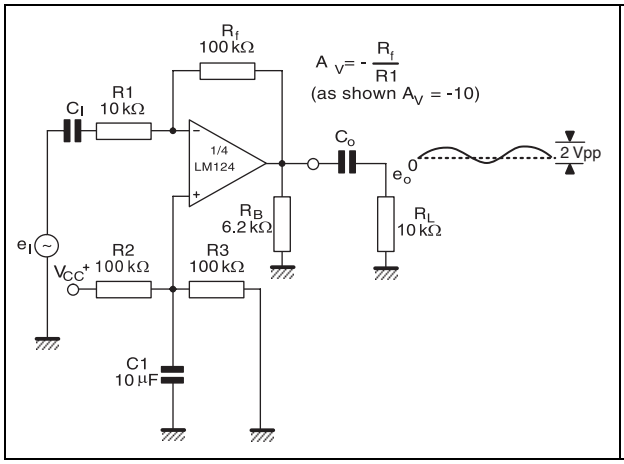


Figure 20. High input Z adjustable gain DC instrumentation amplifier

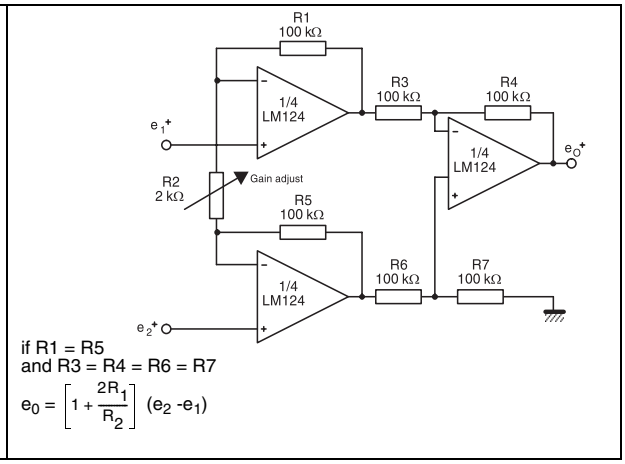


Figure 21. AC coupled non inverting amplifier

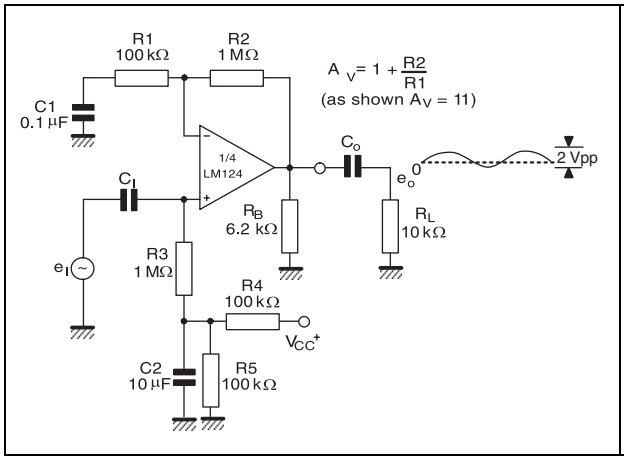


Figure 22. DC summing amplifier

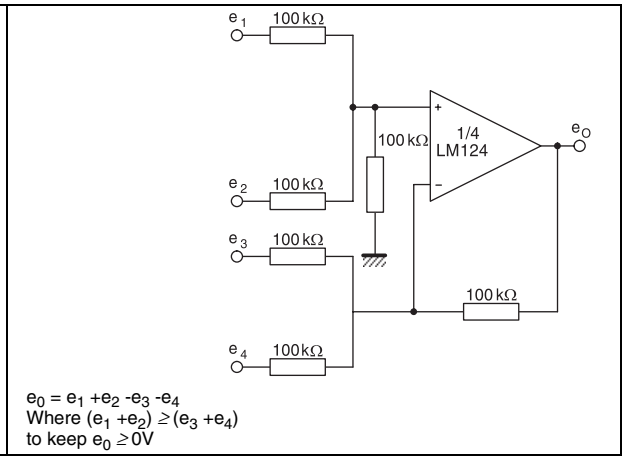


Figure 23. Non-inverting DC gain

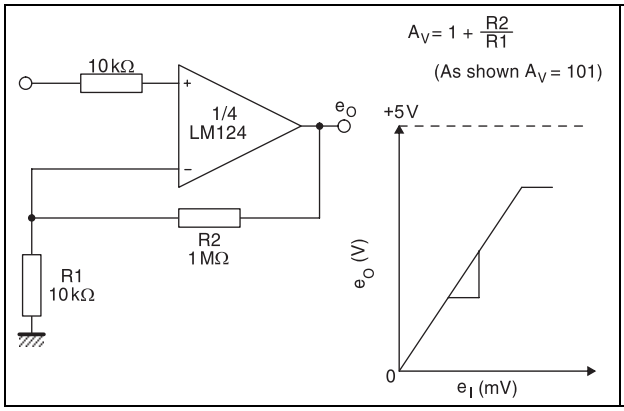


Figure 24. Low drift peak detector

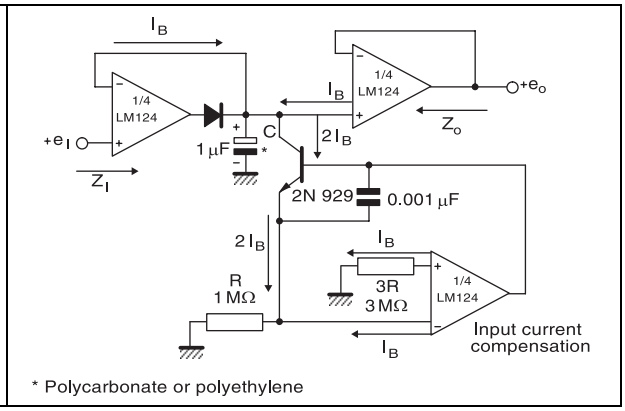


Figure 25. Active bandpass filter

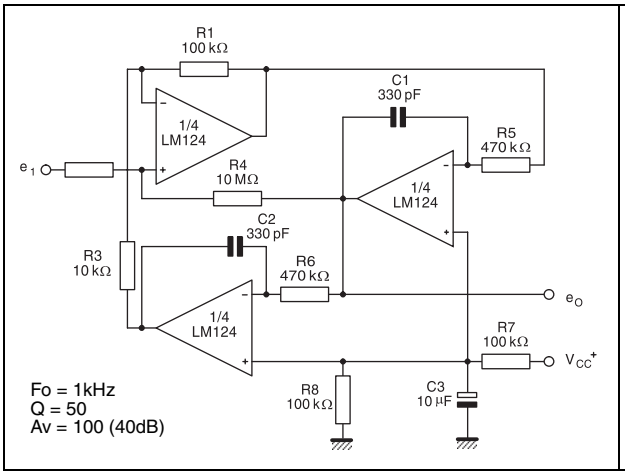


Figure 26. High input Z, DC differential amplifier

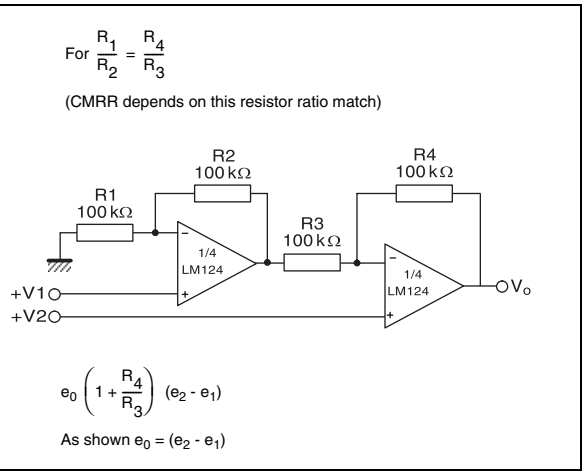
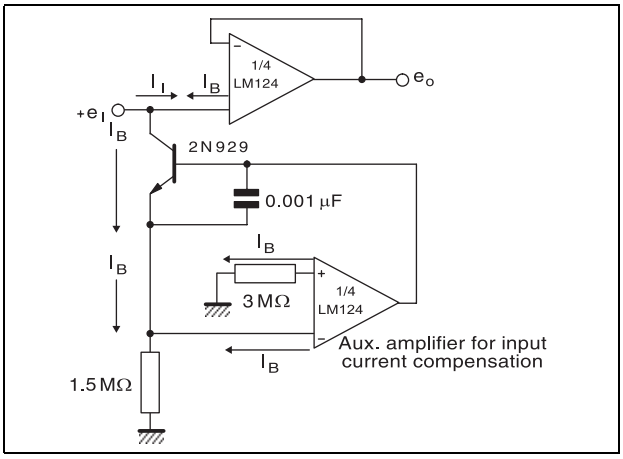


Figure 27. Using symmetrical amplifiers to reduce input current (general concept)



Order codes

Part number	Temperature range	Package	Packing
LM124N	-55°C, +125°C	DIP14	Tube
LM124D/DT		SO-14	Tube or tape & reel
LM224N	-40°C, +105°C	DIP14	Tube
LM224D/DT		SO-14	Tube or tape & reel
LM224PT		(Thin shrink outline package)	Tape & reel
LM324N	0°C, +70°C	DIP14	Tube
LM324D/DT		SO-14	Tube or tape & reel
		(Thin shrink outline package)	Tape & reel

6.1 DIP14 package information

Figure 28. DIP14 package mechanical drawing

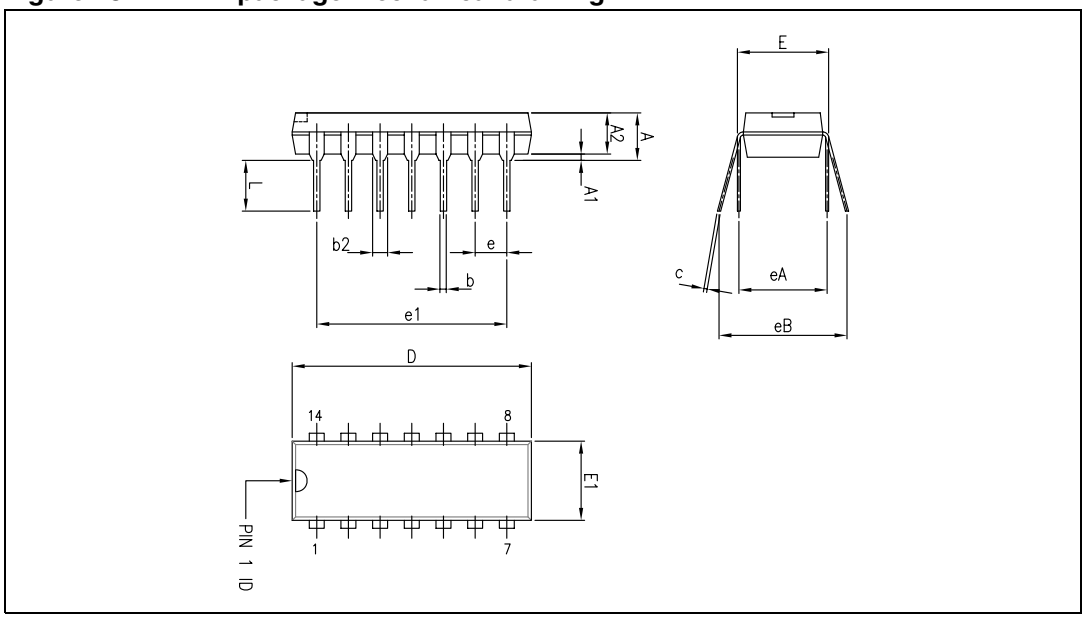


Table 4. DIP14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.33			0.21
A1	0.38			0.015		
A2	2.92	3.30	4.95	0.11	0.13	0.19
b	0.36	0.46	0.56	0.014	0.018	0.022
b2	1.14	1.52	1.78	0.04	0.06	0.07
c	0.20	0.25	0.36	0.007	0.009	0.01
D	18.67	19.05	19.69	0.73	0.75	0.77
E	7.62	7.87	8.26	0.30	0.31	0.32
E1	6.10	6.35	7.11	0.24	0.25	0.28
e		2.54			0.10	
e1		15.24			0.60	
eA		7.62			0.30	
eB			10.92			0.43
L	2.92	3.30	3.81	0.11	0.13	0.15

6.2 SO-14 package information

Figure 29. SO-14 package mechanical drawing

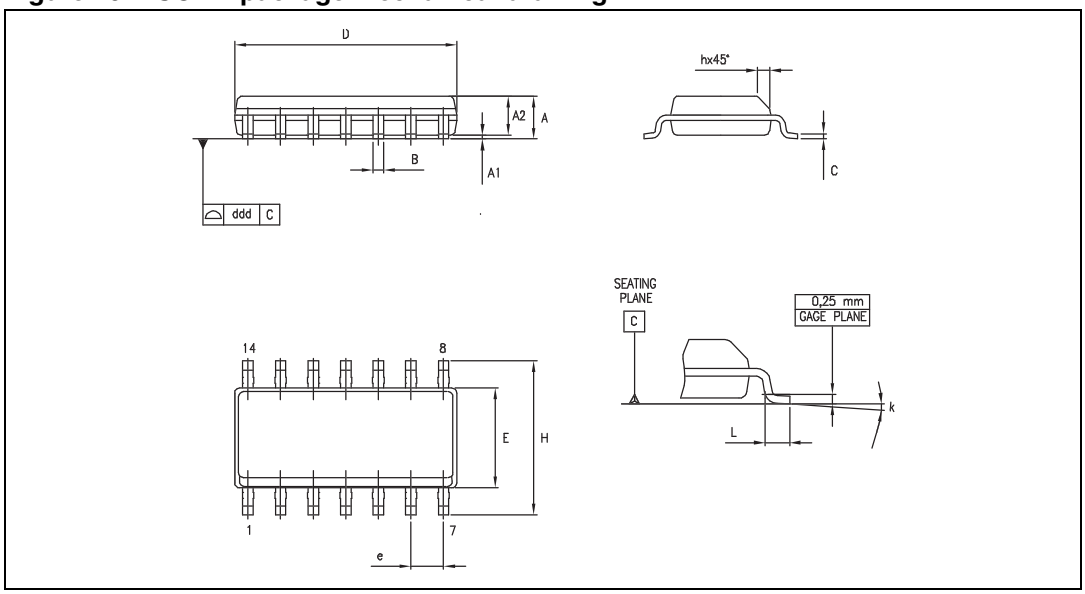


Table 5. SO-14 package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.35		1.75	0.05		0.068
A1	0.10		0.25	0.004		0.009
A2	1.10		1.65	0.04		0.06
B	0.33		0.51	0.01		0.02
C	0.19		0.25	0.007		0.009
D	8.55		8.75	0.33		0.34
E	3.80		4.0	0.15		0.15
e		1.27			0.05	
H	5.80		6.20	0.22		0.24
h	0.25		0.50	0.009		0.02
L	0.40		1.27	0.015		0.05
k	8° (max.)					
ddd			0.10			0.004