Application Notes: SY6982E

High Efficiency, 2A, Two-Cell Boost Li-Ion Battery Charger

General Description

SY6982E is a 3.6-5.5V_{IN}, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout for safety battery charge operation and a programmable input voltage threshold for adaptive input current limit. SY6982E can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

SY6982E along with small QFN3x3 footprint provides small PCB area application.

Ordering Information

SY6982 □(□□)□

- **Temperature Code**
- **Package Code**
- **Optional Spec Code**

Ordering Number	Package type	Note
SY6982EQDC	QFN3x3-16	

Features

Low Profile QFN3x3 Package

- Integrated Synchronous Boost with 18V Rating
- Low R_{DSON} FETs for High Charge Efficiency
- Trickle Current / Constant Current / Constant Voltage Charge Mode
- Programmable Input Voltage Threshold for Adaptive Current Limit.
- Maximum 2A Constant Charge Curre t
- Charge Current Information Indication.
- Programmable Charge Timeout
- Programmable Constant Charge Current
- Selectable Constant Voltage
- ±0.5% Battery Voltage Accuracy
- Thermal Regulation Pr tection
- External Shutdown Function
- Input Voltage UVLO and OVP
- Over Temp rature Protection
- Output Sho t Circuit Protection
- Charge St tus Indication
- Normal Synchronous Boost Operation When Battery Removed

Applications

- Cellular Telephones, PDA, MP3 Players, MP4 Players

Digital Cameras

Bluetooth Applications

- PSP Game Players, NDS Game Players
- Notebook

Typical Applications

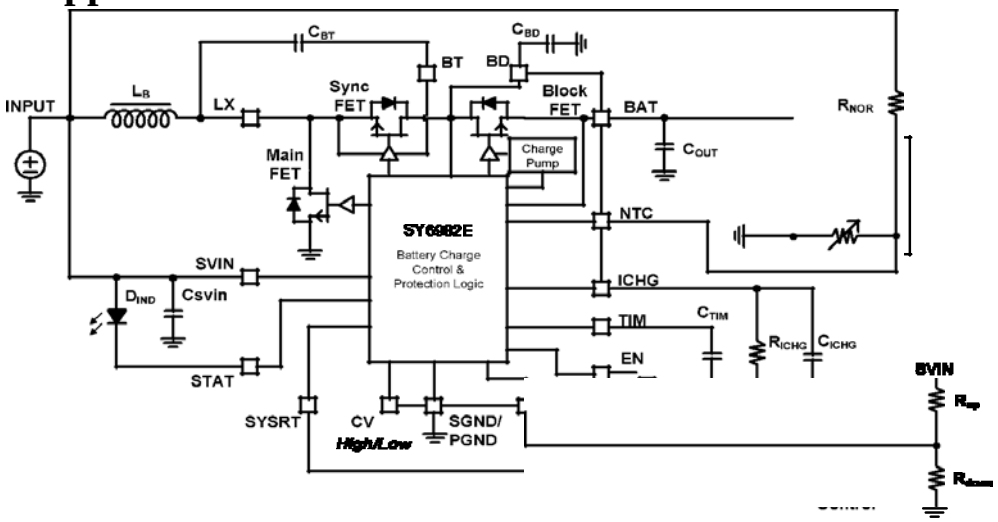
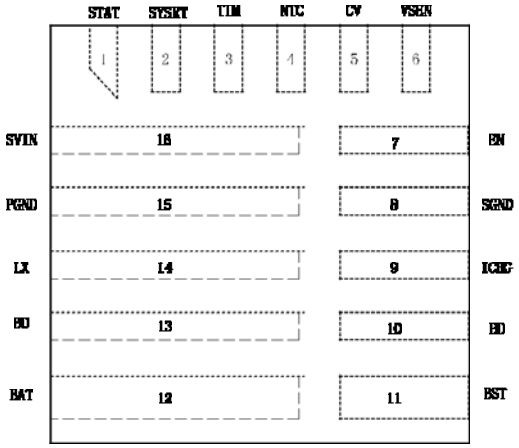


Figure1. Schematic Diagram

Pinout (top view)



(QFN3x3-16)

Top Mark: **AWF*xyz***, (Device code: AWF, ***x=year code, y=week code, z= l t number code***)

Name	Pin Number	Description
STAT	1	Charge status indication pin. It is open drain output pin and pull high to SVIN thru a LED to indicate the charge in process. When the cha ge is done, LED is off.
SYSRT	2	System ON/OFF control pin. When V_{BAT} is lower than 6V, SYSRT pin outputs low logic to turn off the system operation; when V_{BAT} is high than 6V, SYSRT pin outputs high logic to turn on the system operation.
TIM	3	Charge time limit pin. Connect this pin with a capacitor to ground. Internal current source charge the capacitor for TC mode and CC mode's charge time limit. TC charge time limit is about 1/9 of CC charge time.
NTC	4	Thermal protection pin. UTP hreshold is typical 75%V_{SVIN} and OTP threshold is typical 30%V_{SVIN}. Pull up to SVIN can disable charge logic and make the IC operate as normal boost regulator. Pull down to ground can shutdown the IC.
CV	5	Battery CV voltage selection pin. Program 2 different CV thresholds by setting different voltage on the pin. The detailed information is shown in description section.
VSEN	6	Voltage sense of SVIN. If the voltage drops to internal 1.195V reference voltage, the SVIN will be clamped to setting value and input current will be limited.
EN	7	Enable control pin. High logic for enable on, and low logic for enable off.
SGND	8	Signal ground pin.
ICHG	9	Charge current program pin, pull down to GND with a Resistor $R_{ICHG.}$ The mirror current about 1/10000 of the blocking FET current will dump into the external RC network thru ICHG pin and compared to the internal reverence 1V. So I_{CC}=(1V/ R_{ICHG})x10000, I_{TC}=(1V/ R_{ICHG})x1000.
BD	10, 13	Connect to the Drain of internal Blocking FET. Bypass at least 4.7uF ceramic cap to GND.
BST	11	Boost-Strap pin. Supply Rectified FET's gate driver. Decouple this pin to LX with 0.1uF ceramic cap.
BAT	12	Battery positive pin.
LX	14	Switch node pin. Connect to external inductor.
PGND	15	Power ground pin.
SVIN	16	Analog power input pin. Connect a MLCC from this pin to ground to decouple high harmonic noise. This pin has OVP and UVLO function to make the charger operate within safe input voltage area.

Absolute Maximum Ratings

STAT, NTC, CV, VSEN, EN, ICHG, BD, BAT, LX, SVIN ---------- 18V
SYSRT, TIM, BST-LX ---------- 4V
LX Pin current continuous ---------- 5A
Power Dissipation, P_D @ T_A = 25°C, QFN3X3 ---------- 2.6W
Package Thermal Resistance
θ_{JA} ---------- 38°C/W
θ_{JC} ---------- 4°C/W
Junction Temperature Range ---------- -40°C to +125°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 125°C

Recommended Operating Conditions

SVIN ---------- 3.6V to 5.5V
STAT, NTC, CV, VSEN, EN, ICHG, BD, BAT, LX, ---------- -0.3V to 16V
SYSRT, TIM ---------- -0.3V to 3.3V
LX Pin current continuous ---------- 5A
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Electrical Characteristics

T_A=25°C, V_{IN}=5V, GND=0V, C_{IN}=4.7uF, L=0.68uH, R_{ICHG}=10kΩ, C_{TIM}=470nF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bias Supply (V_{SVIN})						
V_{SVIN}	Supply voltage		3.6		16	V
V_{UVLO}	V_{SVIN} under voltage lockout threshold	V_{SVIN} rising and measured from V_{SVIN} to GND			3.6	V
ΔV_{UVLO}	V_{SVIN} under voltage lockout hysteresis	Measured from V_{SVIN} to GND		100		mV
V_{OVP}	Input overvoltage protection	V_{SVIN} rising and measured from V_{SVIN} to GND	5.8			V
ΔV_{OVP}	Input overvoltage protection hysteresis	Measured from V_{SVIN} to GND		0.5		V
Quiescent Current						
I_{BAT}	Battery discharge current	Shutdown IC, EN=NTC=0			10	uA
I_{IN}	Input quiescent current	Disable Charge, EN=1,NTC=0			1.5	mA
Oscillator and PWM						
f_{SW}	Switching frequency			1000		kHz
t_{MINOFF}	Main N-FET minimum off time	With 18V rating		100		ns
t_{MAXOFF}	Main N-FET maximum off time	With 18V rating		30		us
t_{MINON}	Main N-FET minimum on time	With 18V rating		100		ns
Power MOSFET						
R_{NFET_M}	$R_{DS(ON)}$ of Main N-FET			80		mΩ
R_{NFET_R}	$R_{DS(ON)}$ of Rectified N-FET			40		mΩ
R_{NFET_B}	$R_{DS(ON)}$ of Blocking N-FET			40		mΩ
Voltage Regulation						
V_{CV}	2-Cell CV charge mode voltage	V_{CV}<1V	8.358	8.40	8.442	V
		V_{CV}>2V	8.656	8.70	8.743	
V_{CVH}	High level logic for CV1/2		2			V
V_{CVL}	Low level logic for CV1/2				1	V
ΔV_{RCH}	2-Cell Recharge Voltage		100	200	300	mV
V_{TRK}	2-cell TC charge mode battery voltage threshold	Rising edge threshold	5.4	5.6	5.8	V
Battery Connect Detection						
V_{DET}	NTC voltage threshold for Battery detect	NTC Falling Edge	85%		95%	V_{SVIN}
t_{DET}	Detect delay time			30		ms
Charge Current						
	Internal charge current accuracy for Constant Current Mode	I_{CC}=1000mA	-10%		10%	
	Internal charge current accuracy for Trickle Current Mode	I_{TC}=100mA	-50%		50%	
I_{TERM}	Termination current	I_{CC}=1000mA	50	100	150	mA
Output Voltage OVP						
V_{OVP}	Output voltage OVP threshold		105%	110%	115%	V_{CV}
Input Voltage Threshold for Adaptive Current Limit						
$V_{Threshold}$	Voltage reference of VSEN		1.171	1.195	1.219	V
Timer						

t_{TC}	Trickle current charge timeout	C_{TIM}=330nF	0.23	0.5	0.67	hour
t_{CC}	Constant current charge timeout		3.0	4.5	6	hour
t_{MC}	Charge mode change delay time			30		ms
t_{TERM}	Termination delay time			30		ms
t_{RCHG}	Recharge time delay			30		ms
Short Circuit Protection						
V_{SHORT}	Output short protection threshold		1.70	2.00	2.30	V
System ON/OFF Control						
V_{HSYSRT}	High logic of system ON/OFF control		2.1			V
V_{LSYSRT}	Low logic of system ON/OFF control				0.6	V
V_{HYSSYS}	Hysteresis for positive and negative edge			100		mV
Linear charger Mode						
I_{LCHG}	Battery Charger current when the blocking FET is in linear mode	$V_{BAT} < V_{SHORT}$		5%		I_{CC}
I_{LPEAK}	Peak linear current when Battery is absent			1		A
V_{BD}	Bus voltage regulation		5.8	6	6.2	V
V_{TRON}	Blocking FET fully turn on threshold $V_{TRON}=V_{BAT}-V_{IN}$	$V_{BAT} > V_{TRK}$		100		mV
Enable ON/OFF Control						
V_{ENH}	High level logic for enable control		1.5			V
V_{ENL}	Low level logic for enable control				0.4	V
Battery Thermal Protection NTC						
UTP	Under temperature protection		70%	75%	80%	V_{SVIN}
	Under temperature protection hysteresis	Fall ng edge		5%		
OTP	Over temperature protection		28%	30%	32%	
	Over temperature protection hysteresis	Rising edge		2%		
Thermal Regulation And Thermal shutdown						
t_{REG}	Thermal regulation threshold	Rising Threshold		120		ºC
T_{REGHYS}	Thermal regulation hysteresis falling edge			20		ºC
	Thermal regulation fold back ratio			0.25		I_{CC}
t_{SD}	Thermal shutdown temperature	Rising Threshold		160		ºC
T_{SDHYS}	Thermal shutdown temperature hysteresis			30		ºC

Note 1: Stresses be ond the “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational s ctions of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a low effective four-layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard.

Note 3: The device is not guaranteed to function outside its operating conditions

General Function Description

SY6982E is a 3.6-5.5V_{IN}, 2A two-cell synchronous boost Li-Ion battery charger integrates 1MHz switching frequency and full protection functions. The charge current up to 2A can be programmed by using the external resistor for different portable applications and indicates the charger current information simultaneous. It also has a programmable charge timeout for safety battery charge operation and a programmable input voltage threshold for adaptive input current limit. SY6982E can disconnect output when there is output short circuit or shutdown happens. It consists of 18V rating FETs with extremely low ON resistance to achieve high charge efficiency and simple peripheral circuit design.

Charging Status Indication Description

1. Charge-In-Process – Pull and keep STAT pin to Low;
2. Charge Done – Pull and keep STAT pin to High;
3. Fault Mode – Output high and low voltage alternatively with 1.3Hz frequency. Connect a LED from SVIN to STAT pin, LED ON means Charge-in-Process, LED OFF means Charge Done, LED Flashing with 1.3HZ means Fault Mode.

Switching Mode Boost Charger Basic Operation Description

Switching Mode Control Strategy

SY6982E is a switching mode Boost charger for the applications with USB power input. The 1MHz fixed frequency is easy for the size minimization of peripheral circuit design.

Operation Principle

SY6982E can normally work with or without Li-Ion battery both.

Battery Present

When the battery is present, SY6982E will works on trickle charging, constant current charging and constant voltage charging mode according to the battery voltage.

Battery Absent

If there's no battery connection detected thru NTC pin, SY6982E operates as a normal switching mode boost converter. The internal constant current loop and voltage loop are active both.

Basic Protection Principle

SY6982E has fully battery charging protect on. When the input over voltage protection, the output over voltage protection, the thermal protection or the timeout protection happens, the b st charger stops switching immediately. When the V_{BAT} is lower than V_{SHORT}, the short circuit p otection happens. The main FET is turned off firstly. The block FET enters linear mode with 1/20 I_{CC} charging current. When V_{BAT} recovers back to be higher than V_{SHORT}, the boost charger restarts to work at light load and regulates V_{BD} at 6V. The line charge current is increased from 1/20 I_{CC} to 1/10 I_{CC}. When V_{BAT} recovers back to be higher than V_{SVIN}, the boost switching charger takes over.

Adaptive Input Current Limit Principle

SY6982E can protect the input DC source from over load by the special loop control. The high charging current will caused a voltage drop at SVIN when the input DC source is over load. When VSEN drops below the internal 1.195V reference, SY6982E will decrease the duty cycle to reduce the charging current.

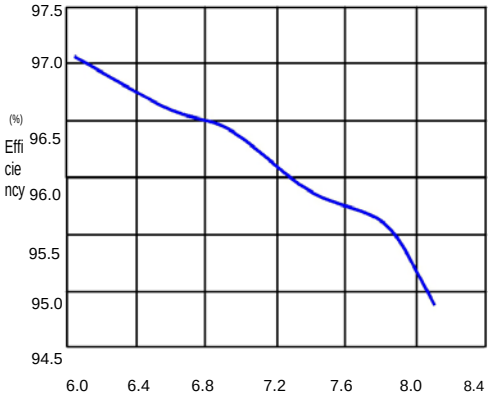
Constant Voltage Threshold Program Principle

SY6982E can program the constant voltage threshold thru the CV pin. When V_{CV} is higher than 2V, the constant voltage threshold is 8.7V; when V_{CV} is lower than 1V, the constant voltage threshold is 8.4V.

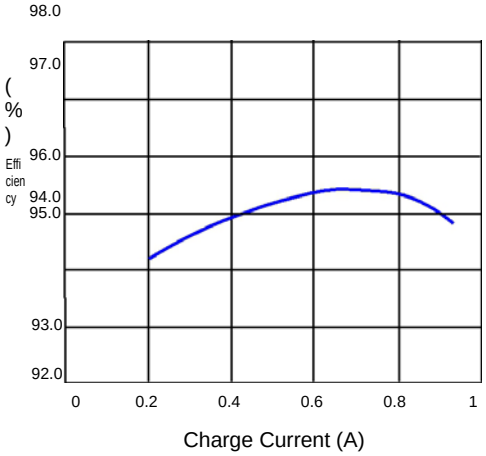
Typical Performance Characteristics

(T_A=25°C, V_{IN}=5V, R_{RCH}=10kΩ, unless otherwise specified.)

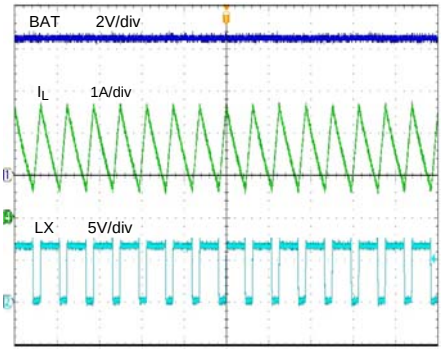
Efficiency vs. Bat voltage (CC mode)



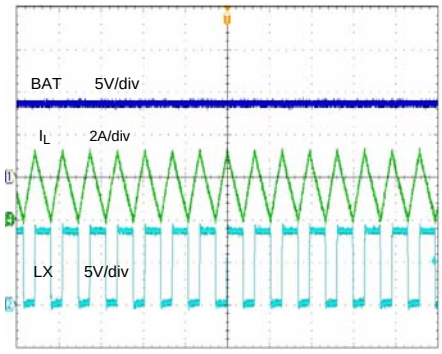
Efficiency vs. Charge current (CV mode)



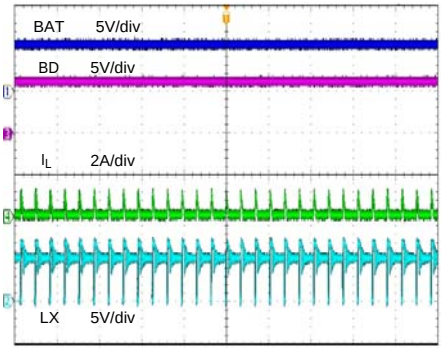
Steady waveform (CC Mode)



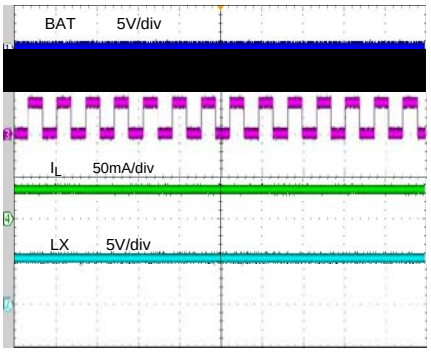
St ady waveform (CV Mode)



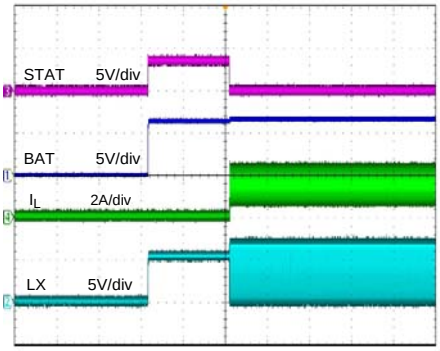
Steady waveform (TC Mode)



Steady waveform (Short Mode)

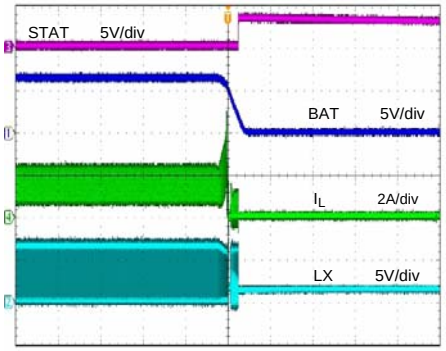


Power On (CC Mode)



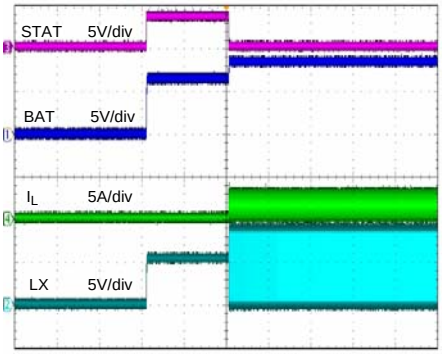
Time (400ms/div)

Power Off (CC Mode)



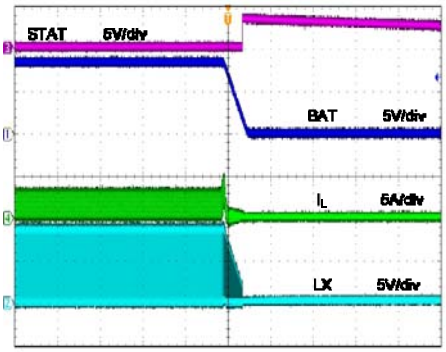
Time (2ms/div)

Power On (CV Mode)



Time (400ms/div)

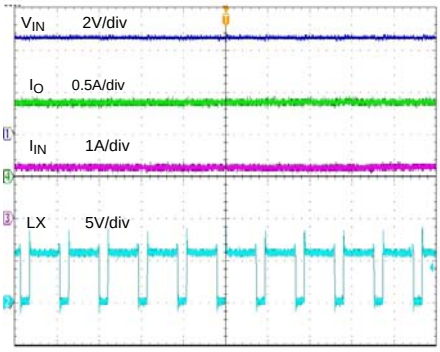
Power Off (CV Mode)



Time (4ms/div)

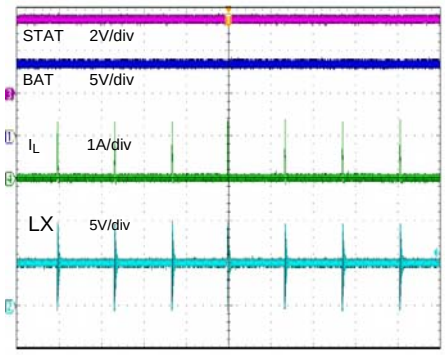
Adaptive input current limit

(5V/1A adapter)



Time (1μs/div)

Boost Mode (Null load)



Time (20μs/div)

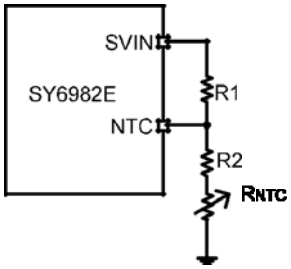
Applications Information

Because of the high integration of SY6982E, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L, NTC resistors R1,R2, input voltage threshold resistors Rup, Rdown and timer capacitor C_{TIM} need to be selected for the targeted applications specifications.

NTC resistor:

SY6982E monitors battery temperature by measuring the input voltage and NTC voltage. The controller triggers the UTP or OTP when the rate K (K= V_{NTC}/V_{SVIN}) reaches the threshold of UTP (K_{UT}) or OTP (K_{OT}). The temperature sensing network is showed as below.

Choose R1 and R2 to program the proper UTP and OTP points.



The calculation steps are:

1. Define K_{UT}, K_{UT} =70~80%
2. Define K_{OT}, K_{OT} =28~32%
3. Assume the resistance of the battery NTC thermistor is R_{UT} at UTP threshold a d R_{OT} at OTP threshold.
4. Calculate R2,

$$R2 = \frac{K_{OT}(1-K_{UT})R_{UT} - K_{UT}(1-K_{OT})R_{OT}}{K_{UT} - K_{OT}}$$

5. Calculate R1

$$R1 = (1/K_{OT} - 1)(R2 + R_{OT})$$

If choose the typical values K_{UT} =75% and K_{OT}=30%, then

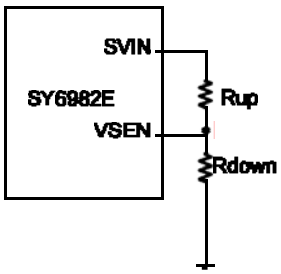
$$R2 = 0.17R_{UT} - 1.17R_{OT}$$

$$R1 = 2.3(R2 + R_{OT})$$

Input Voltage Threshold VSEN for Adaptive Current Limit.

SY6982E monitors input voltage by measuring the VSEN voltage, when VSEN drops below the internal 1.195V reference, SY6982E will decrease the duty cycle to reduce the charging current.

The input voltage sense network shows below, choose Rup,Rdown to set the input voltage threshold V_{INT}:



$$V_{INT} = \frac{V_{SEN}*(R_{down} + R_{up})}{R_{down}}$$ Unit:V

V_{SEN} is 1.195V.

Timer capacitor C_{TIM}

The charger also provides a programmable charge timer. The charge time is programmed by the capacitor connected between the TIM pin and GND. The ca acitance is given by the formula:

$C_{TIM}=2*10^{-11}T_{CC}$ Unit:F

T_{CC} is the target constant charge time, unit: s.

Input capacitor C_{IN}:

The ripple current through input capacitor is greater than

$$I_{CIN\_RMS} = \frac{V_{IN}*(V_{OUT} - V_{IN})}{2\sqrt{3} * L*F_{SW} * V_{OUT}}$$

X5R or X7R ceramic capacitors with greater than 4.7uF capacitance are recommended to handle this ripple current.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. This ripple voltage is related to the capacitance and its equivalent series resistance (ESR). For the best performance, it is recommended to use X5R or better grade low ESR ceramic capacitor. The voltage rating of the output capacitor should be higher than the maximum output voltage. The minimum required capacitance can be calculated as:

$$C_{OUT} = \frac{I_{CC}*(V_{OUT} - V_{IN})}{F_{SW} \times V_{OUT} \times V_{RIPPLE}}$$

V_{RIPPLE} is the peak to peak output ripple, I_{CC} is the setting charge current.

For SY6982E, output capacitor is paralleled by C_{BD} and C_{BAT}, for smaller output ripple noise, each

capacitor with greater than 10uF capacitance is recommended.

Inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the average input current. The inductance is calculated as:

$$L = \frac{V_{IN}}{V_{OUT}} \frac{^{2}(V_{OUT} - V_{IN})}{I_{CC} \times F_{SW} \times 40\%}$$

Where F_{SW} is the switching frequency and I_{CC} is the setting charge current.

The SY6982E is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

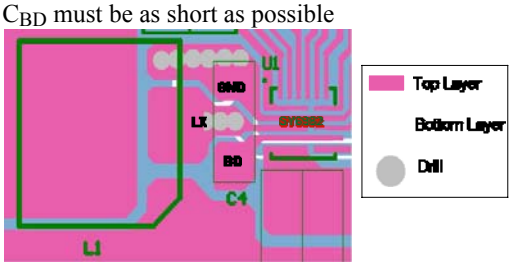
$$I_{SAT,MIN} > \frac{V_{OUT}}{V_{IN}} \times I_{CC} + \frac{V_{IN}}{V_{OUT}} \times \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mohm to achieve a good overall efficiency.

Layout Design:

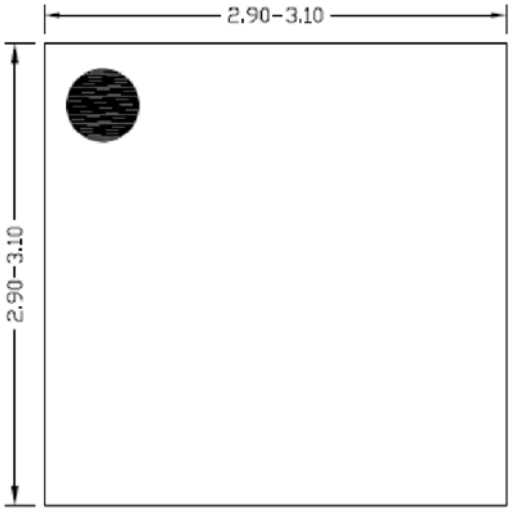
The layout design of SY6982E regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: C_{SVIN}, L, C_{BD}.

1) The loop of main MOSFET, rectifier diode, and C_{BD} must be as short as possible

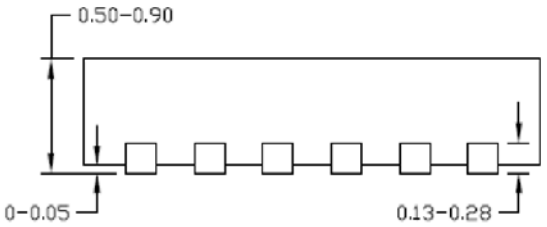


2) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance.
3) C_{SVIN} must be close to pin SVIN and GND.
4) The PCB copper area associated with LX pin must be minimized to avoid the potential noise probl m.
5) The small signal components R_{ICHG} ,Rup and Rdown must be placed close to IC and must not be adjacent to the LX net on the PCB layout to avoid the noise problem.

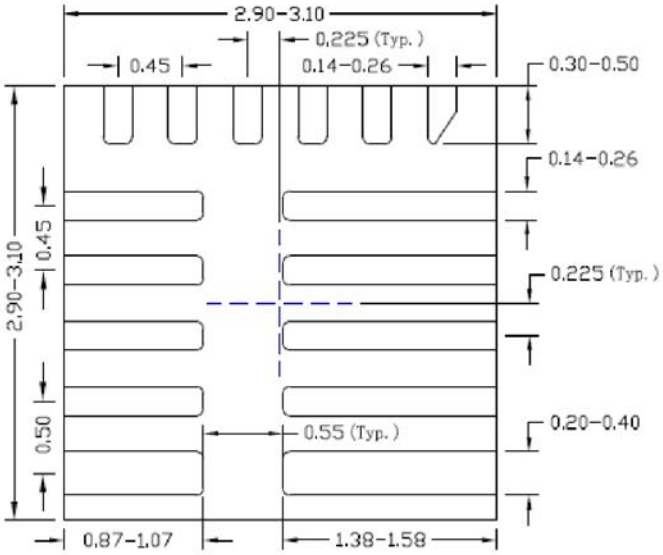
QFN3x3-16 Package Outline Drawing



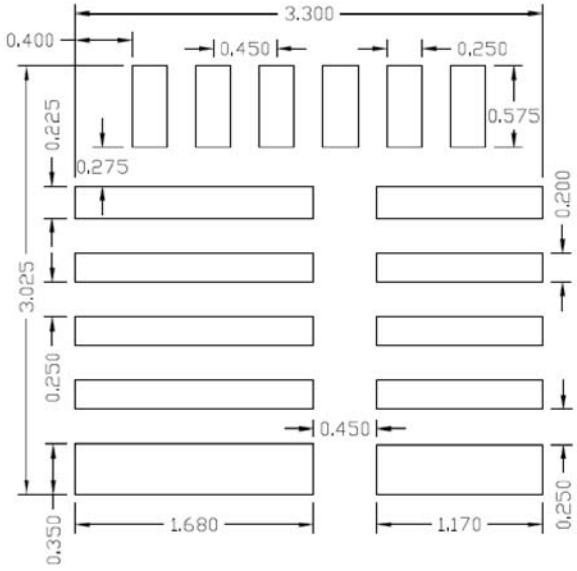
Top View



Side View



Bottom View



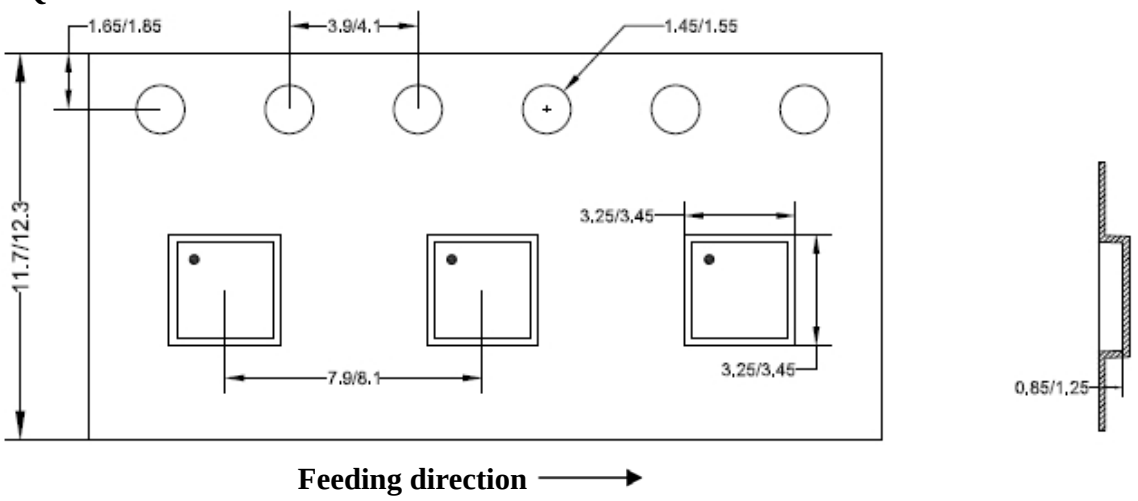
Recommended PCB layout (Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr**

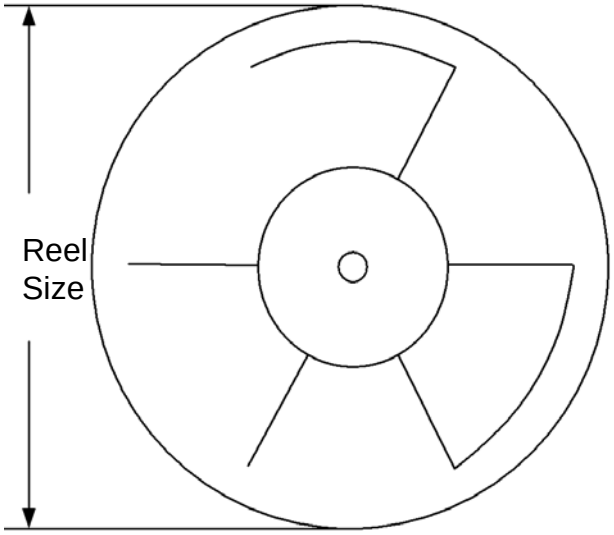
Taping & Reel Specification

1. Taping orientation

QFN3x3



2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN3x3	12	8	13"	400	400	5000

3. Others: NA