74LVCU04A-Q100

Hex unbuffered inverter

Rev. 1 — 21 September 2016

Product data sheet

1. General description

The 74LVCU04A-Q100 is a general purpose hex unbuffered inverter. Each of the six inverters is a single stage with unbuffered outputs.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - ◆ Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ MIL-STD-883, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

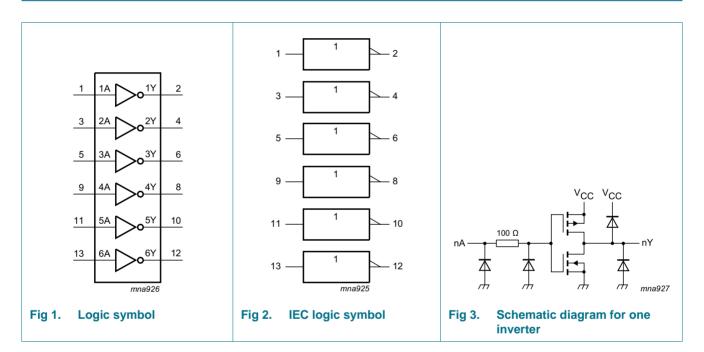


3. Ordering information

Table 1. Ordering information

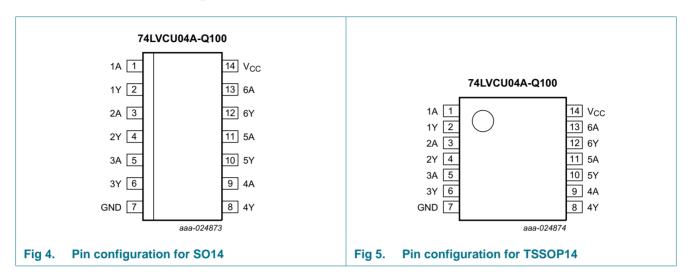
Type number	Package						
	Temperature range	Name	Description	Version			
74LVCU04AD-Q100	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1			
74LVCU04APW-Q100	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1			

4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table[1]

Input nA	Output nY
L	Н
Н	L

[1] H = HIGH voltage level; L = LOW voltage level

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		<u>[1]</u>	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
Vo	output voltage		[2]	-0.5	V _{CC} + 0.5	V
I _O	output current	$V_O = 0 \text{ V to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	<u>[3]</u>	-	500	mW

^[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
	rate	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

^[2] The output voltage ratings may be exceeded if the output current ratings are observed.

^[3] For SO14 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K. For TSSOP14 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	–40 °C to +85 °C			+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level	$V_{OL(max)} = 0.5 \text{ V}; I_{O} = -100 \mu\text{A}$						
	input voltage	V _{CC} = 1.2 V	1.08	-	-	1.12	-	V
		V _{CC} = 1.65 V to 1.95 V	1.3	-	-	1.5	-	V
		V _{CC} = 2.3 V to 2.7 V	1.8	-	-	2.0	-	V
		V _{CC} = 3.0 V	2.0	-	-	2.4	-	V
		V _{CC} = 3.6 V	2.4	-	-	2.8	-	V
V_{IL}	LOW-level input voltage	$V_{OH(min)} = V_{CC} - 0.5 \text{ V};$ $I_O = -100 \mu A$						
		V _{CC} = 1.2 V	-	-	0.12	-	0.1	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.6	-	0.4	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.5	V
		V _{CC} = 3.0 V	-	-	1.0	-	0.6	V
		V _{CC} = 3.6 V	-	-	1.2	-	0.7	V
V _{OH}	HIGH-level	V _I = GND						
	output voltage	$V_{CC} = 3.0 \text{ V}; I_{O} = -100 \mu\text{A}$	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		$V_{CC} = 1.65 \text{ V}; I_{O} = -4 \text{ mA}$	1.2	-	-	1.05	-	V
		$V_{CC} = 2.3 \text{ V}; I_{O} = -8 \text{ mA}$	1.8	-	-	1.65	-	V
		$V_{CC} = 2.7 \text{ V}; I_{O} = -12 \text{ mA}$	2.2	-	-	2.05	-	V
		$V_{CC} = 3.0 \text{ V}; I_{O} = -18 \text{ mA}$	2.4	-	-	2.25	-	V
		$V_{CC} = 3.0 \text{ V}; I_{O} = -24 \text{ mA}$	2.2	-	-	2.0	-	V
V _{OL}	LOW-level	$V_I = V_{CC}$						
	output voltage	$V_{CC} = 3.0 \text{ V}; I_{O} = 100 \mu\text{A}$	-	-	0.20	-	0.60	V
	voltage	$V_{CC} = 1.65 \text{ V}; I_{O} = 4 \text{ mA}$	-	-	0.45	-	0.65	V
		$V_{CC} = 2.3 \text{ V}; I_{O} = 8 \text{ mA}$	-	-	0.60	-	0.80	V
		$V_{CC} = 2.7 \text{ V}; I_{O} = 12 \text{ mA}$	-	-	0.40	-	0.30	V
		$V_{CC} = 3.0 \text{ V}; I_{O} = 24 \text{ mA}$	-	-	0.55	-	0.80	V
lı	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$	-	±0.1	±5	-	±20	μΑ
lcc	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND};$ $I_O = 0 \text{ A}$	-	0.1	10	-	40	μА
∆l _{CC}	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_{I} = V_{CC} - 0.6 \text{ V};$ $I_{O} = 0 \text{ A}$	-	5	500	-	5000	μА
Cı	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$	-	5.5	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 9.

Symbol	Parameter	Conditions	Conditions		-40 °C to +85 °C			o +125 °C	Unit
				Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Figure 6	[2]						
		V _{CC} = 1.2 V		-	6.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V		0.3	3.7	7.8	0.3	9.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$		0.5	2.2	4.4	0.5	5.2	ns
		V _{CC} = 2.7 V		0.5	2.0	4.5	0.5	6.0	ns
		V _{CC} = 3.0 V to 3.6 V		0.5	2.0	4.0	0.5	5.0	ns
t _{sk(o)}	output skew time	V _{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	-	1.5	ns
C _{PD}	power dissipation	per inverter; $V_I = GND$ to V_{CC}	[4]						
	capacitance	V _{CC} = 1.65 V to 1.95 V		-	2.3	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V		-	5.5	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$		-	8.4	-	-	-	pF

- [1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.2$ V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

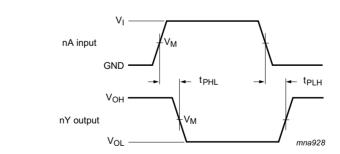
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

11. Waveforms



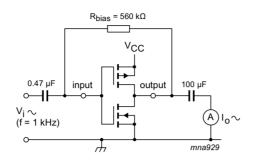
 $V_{M} = 1.5 \text{ V at } V_{CC} \ge 2.7 \text{ V};$

 $V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7 \text{ V}$;

 V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. Input (nA) to output (nY) propagation delays

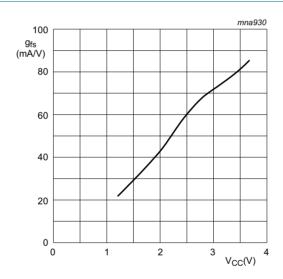
74LVCU04A Q100



$$g_{fs} = \frac{dI_O}{dV_I}; at \ constant \ V_O$$

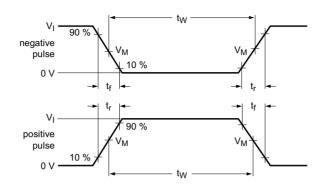
f_i = 1 kHz at V_O is constant

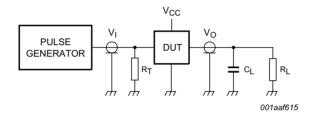
Fig 7. Test setup for measuring forward transconductance



 $T_{amb} = 25 \, ^{\circ}C$

Fig 8. Typical forward transconductance as a function of supply voltage





Test data is given in Table 8.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

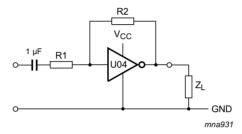
Supply voltage	upply voltage Input		Load		
	V _I	t _r , t _f	C _L	R _L	
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ	
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω	
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	

12. Application information

12.1 Application diagrams

Some applications for the 74LVCU04A-Q100 are:

- Linear amplifier: see Figure 10
- Crystal oscillator designs; see Figure 11
- Astable multivibrator; see Figure 12



 $V_{o(p-p)} = V_{CC} - 1.5 \text{ V}$ centered at $0.5V_{CC}$.

$$A_u = -\frac{G_{OL}}{I + \frac{RI}{R2}(I + G_{OL})}$$

 G_{OL} = loop gain.

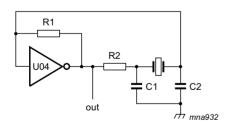
 A_u = voltage amplification.

 $R1 \ge 3 \text{ k}\Omega, R2 \le 1 \text{ M}\Omega$

 $Z_L > 10 \text{ k}\Omega; A_{OL} = 20 \text{ (typ.)}$

Typical unity gain bandwidth product is 5 MHz.

Fig 10. 74LVCU04A-Q100 used as linear amplifier



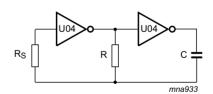
 $C_1 = 47 pF (typical)$

 $C_2 = 22 pF (typical)$

 $R_1 = 1$ to 10 $M\Omega$ (typical)

 R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 2 mA at V_{CC} = 3 V and f = 1 MHz)

Fig 11. 74LVCU04A-Q100 used as crystal oscillator



$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

 $R_S \approx 2R$.

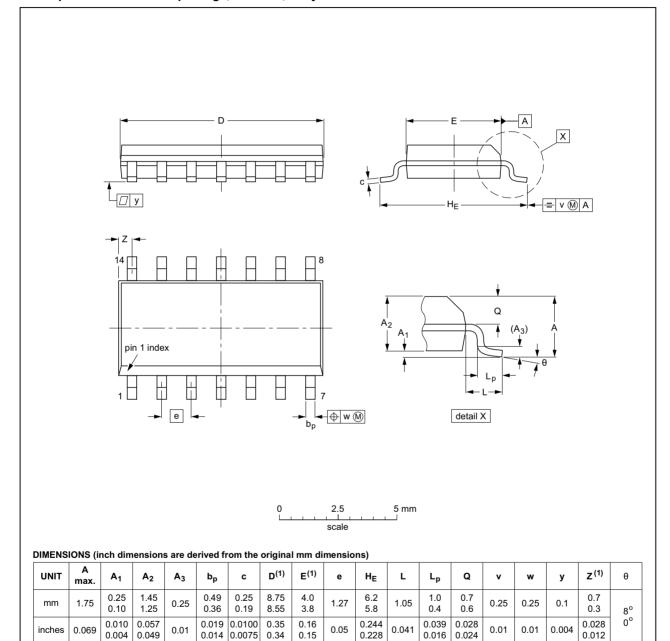
The average I_{CC} is approximately 3.5 + 0.05f (MHz) \times C (pF) [mA] at V_{CC} = 3.0 V.

Fig 12. 74LVCU04A-Q100 used as astable multivibrator

13. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Note

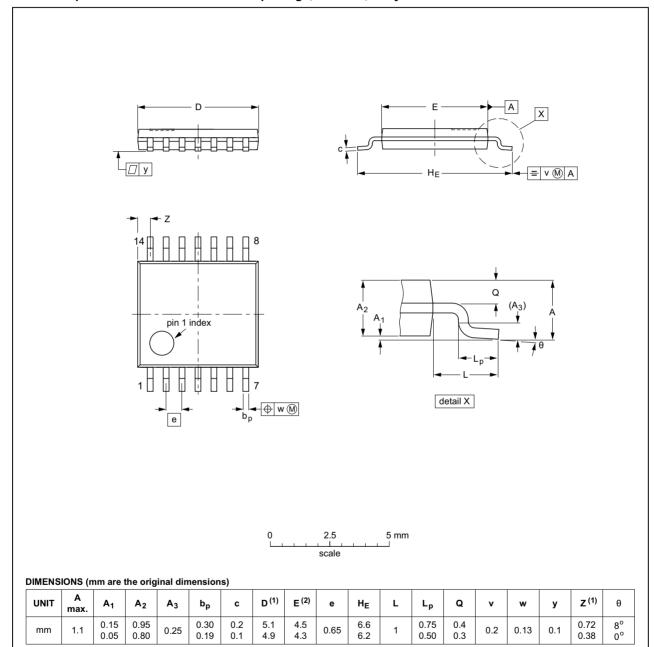
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT108-1	076E06	MS-012				99-12-27 03-02-19

Fig 13. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFERENCES			EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE
SOT402-1		MO-153				99-12-27 03-02-18

Fig 14. Package outline SOT402-1 (TSSOP14)

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic
MIL	Military

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVCU04A_Q100 v.1	20160921	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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18. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	
5.1	Pinning	3
5.2	Pin description	3
6	Functional description	3
7	Limiting values	4
8	Recommended operating conditions	4
9	Static characteristics	5
10	Dynamic characteristics	6
11	Waveforms	6
12	Application information	9
12.1	Application diagrams	9
13	Package outline	. 10
14	Abbreviations	. 12
15	Revision history	. 12
16	Legal information	. 13
16.1	Data sheet status	
16.2	Definitions	. 13
16.3	Disclaimers	. 13
16.4	Trademarks	. 14
17	Contact information	. 14
10	Contents	15

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