

74LVC16244A; 74LVCH16244A

16-bit buffer/line driver; 5 V input/output tolerant; 3-state

Rev. 15 — 15 February 2019

Product data sheet

1. General description

The 74LVC16244A; 74LVCH16244A are 16-bit non-inverting buffer/line drivers with 3-state bus compatible outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. It features four output enable inputs, (1OE to 4OE) each controlling four of the 3-state outputs. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state.

Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications.

The 74LVCH16244A bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

2. Features and benefits

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- High-impedance when $V_{CC} = 0$ V
- All data inputs have bus hold. (74LVCH16244A only)
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-B exceeds 200 V
 - CDM ANSI/ESDA/Jedec JS-002 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74LVC16244ADL	-40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVCH16244ADL				
74LVC16244ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVCH16244ADGG				
74LVC16244ADGV	-40 °C to +125 °C	TSSOP48 [1]	plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm	SOT480-1
74LVCH16244ADGV				

[1] Also known as TVSOP48.

4. Functional diagram

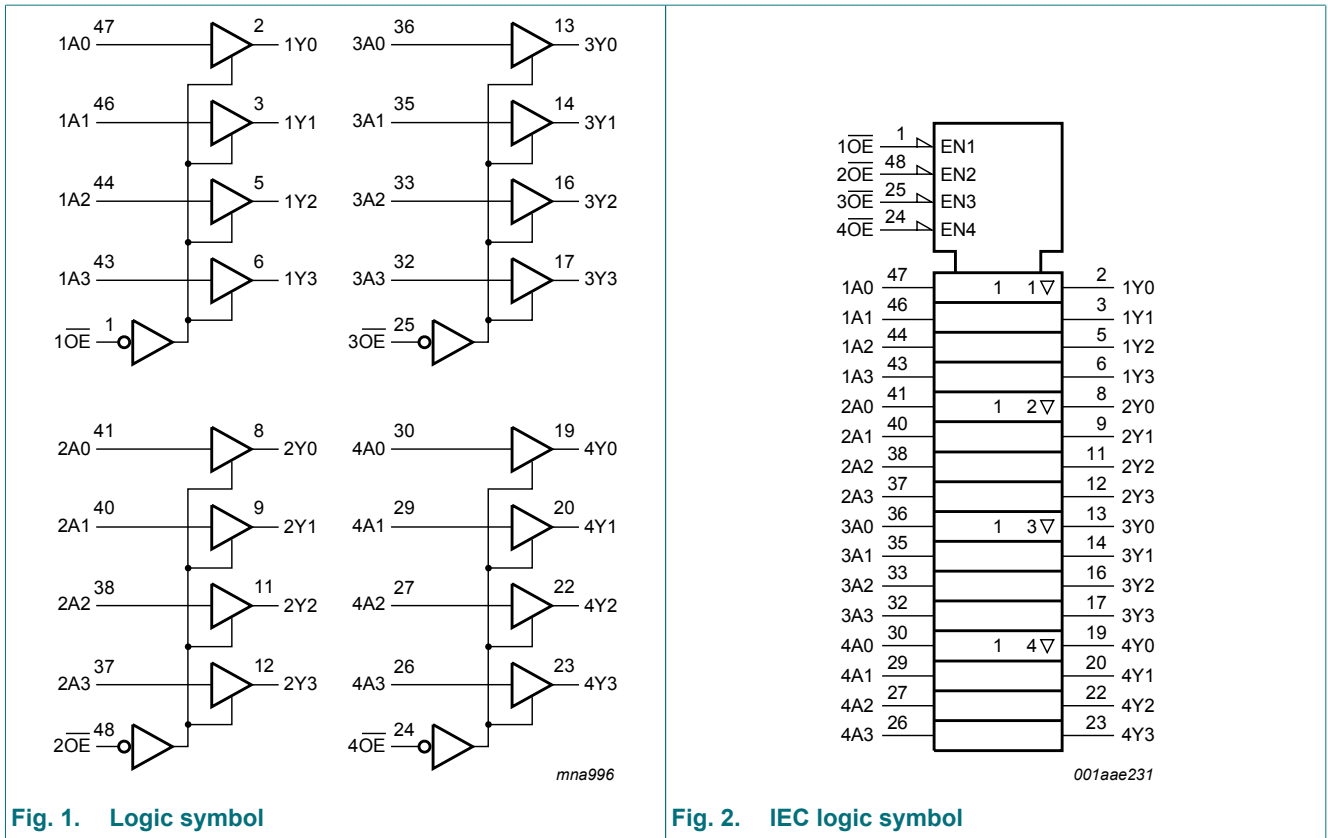


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

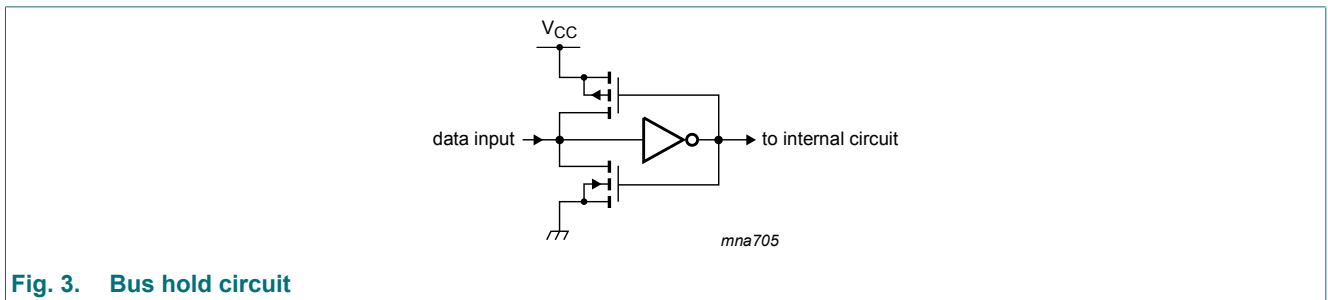


Fig. 3. Bus hold circuit

5. Pinning information

5.1. Pinning

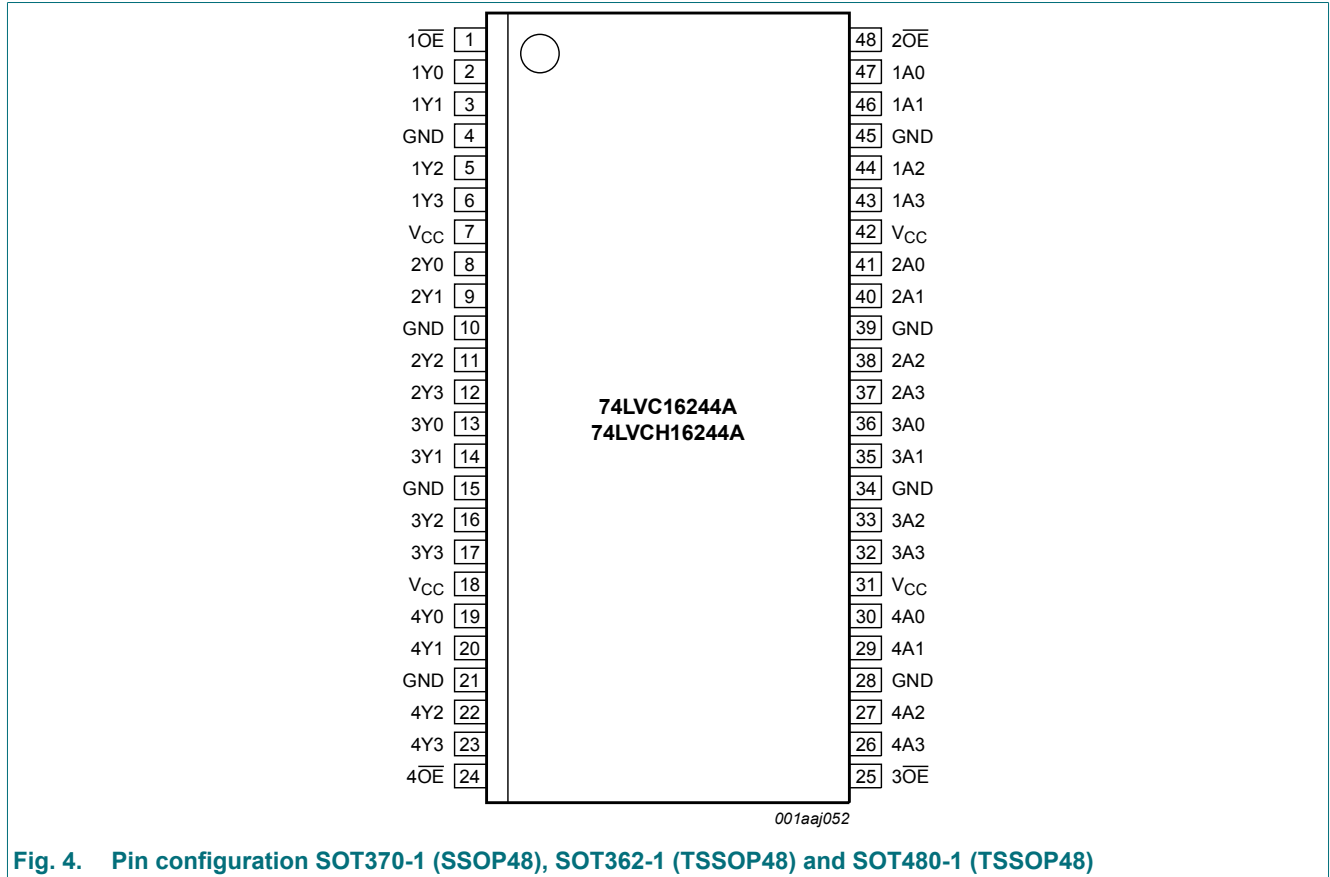


Fig. 4. Pin configuration SOT370-1 (SSOP48), SOT362-1 (TSSOP48) and SOT480-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 48, 25, 24	output enable input (active LOW)
1Y0 to 1Y3	2, 3, 5, 6	data output
2Y0 to 2Y3	8, 9, 11, 12	data output
3Y0 to 3Y3	13, 14, 16, 17	data output
4Y0 to 4Y3	19, 20, 22, 23	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V _{CC}	7, 18, 31, 42	supply voltage
1A0 to 1A3	47, 46, 44, 43	data input
2A0 to 2A3	41, 40, 38, 37	data input
3A0 to 3A3	36, 35, 33, 32	data input
4A0 to 4A3	30, 29, 27, 26	data input

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage		[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	output HIGH or LOW	[2] -0.5	V _{CC} + 0.5	V
		output 3-state	[2] -0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C; [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	3.6	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW	0	-	V _{CC}	V
		output 3-state	0	-	5.5	V
T _{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 µA; V _{CC} = 1.65 V to 3.6 V	V _{CC} -0.2	-	-	V _{CC} -0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 µA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	µA
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND [2]	-	±0.1	±5	-	±20	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; I _O = 0 A; V _I = V _{CC} or GND	-	0.1	20	-	80	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF
I _{BHL}	bus hold LOW current	V _{CC} = 1.65; V _I = 0.58 V [3] [4]	10	-	-	10	-	µA
		V _{CC} = 2.3; V _I = 0.7 V	30	-	-	25	-	µA
		V _{CC} = 3.0; V _I = 0.8 V	75	-	-	60	-	µA
I _{BHH}	bus hold HIGH current	V _{CC} = 1.65; V _I = 1.07 V [3] [4]	-10	-	-	-10	-	µA
		V _{CC} = 2.3; V _I = 1.7 V	-30	-	-	-25	-	µA
		V _{CC} = 3.0; V _I = 2.0 V	-75	-	-	-60	-	µA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
I _{BHLO}	bus hold LOW overdrive current	V _{CC} = 1.95 V [3] [5]	200	-	-	200	-	µA
		V _{CC} = 2.7 V	300	-	-	300	-	µA
		V _{CC} = 3.6 V	500	-	-	500	-	µA
I _{BHHO}	bus hold HIGH overdrive current	V _{CC} = 1.95 V [3] [5]	-200	-	-	-200	-	µA
		V _{CC} = 2.7 V	-300	-	-	-300	-	µA
		V _{CC} = 3.6 V	-500	-	-	-500	-	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

[2] The bus hold circuit is switched off when V_I > V_{CC} allowing 5.5 V on the input terminal.

[3] Valid for data inputs only. Control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data input holds the input below the specified V_I level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nYn; see Fig. 5 [2]						
		V _{CC} = 1.2 V	-	11.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	4.8	10.7	1.5	11.3	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	5.3	1.0	5.9	ns
		V _{CC} = 2.7 V	1.0	2.6	4.7	1.0	6.0	ns
t _{en}	enable time	nOE to nYn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	15.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	6.2	12.1	1.5	12.7	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.5	6.4	1.0	7.1	ns
		V _{CC} = 2.7 V	1.0	3.3	5.8	1.0	7.5	ns
t _{dis}	disable time	nOE to nYn; see Fig. 6 [2]						
		V _{CC} = 1.2 V	-	10.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	4.4	8.7	2.5	9.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.4	4.9	1.0	5.3	ns
		V _{CC} = 2.7 V	1.0	3.2	6.2	1.0	8.0	ns
C _{PD}	power dissipation capacitance	per input; V _I = GND to V _{CC} [3]						
		V _{CC} = 1.65 V to 1.95 V	-	4.8	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	8.3	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	11.4	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.

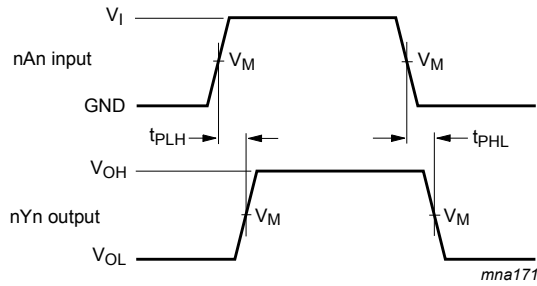
[2] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW). P_D = C_{PD} × V_{CC}² × f_i × N + ∑(C_L × V_{CC}² × f_o) where:

f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts; N = number of inputs switching; ∑(C_L × V_{CC}² × f_o) = sum of the outputs.

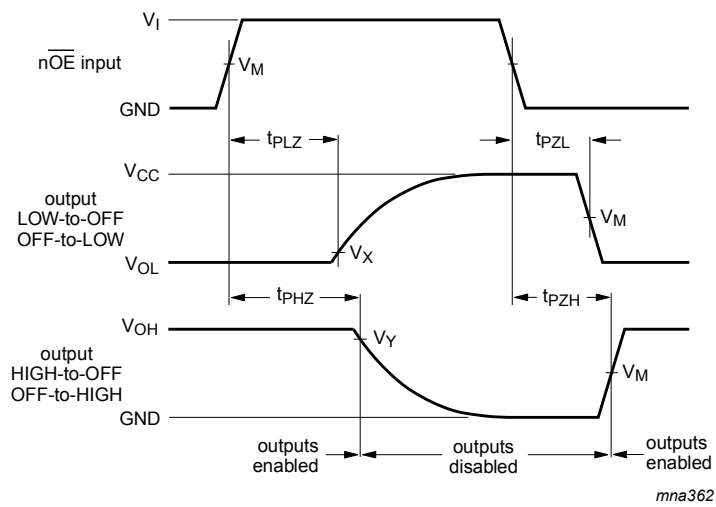
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. The input (nAn) to output (nYn) propagation delays



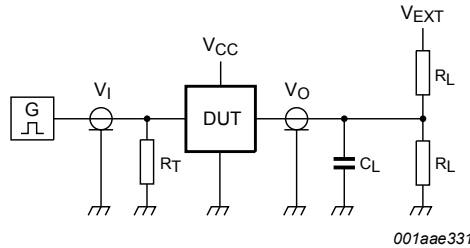
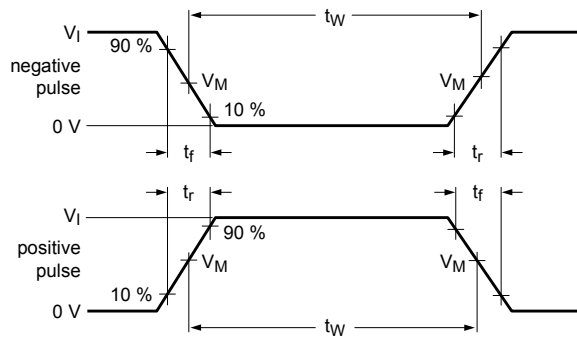
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_M	V_I	V_M	V_X	V_Y
1.2 V	$0.5 \times V_{CC}$	V_{CC}	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$0.5 \times V_{CC}$	V_{CC}	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	V_{CC}	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	1.5 V	2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	1.5 V	2.7 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

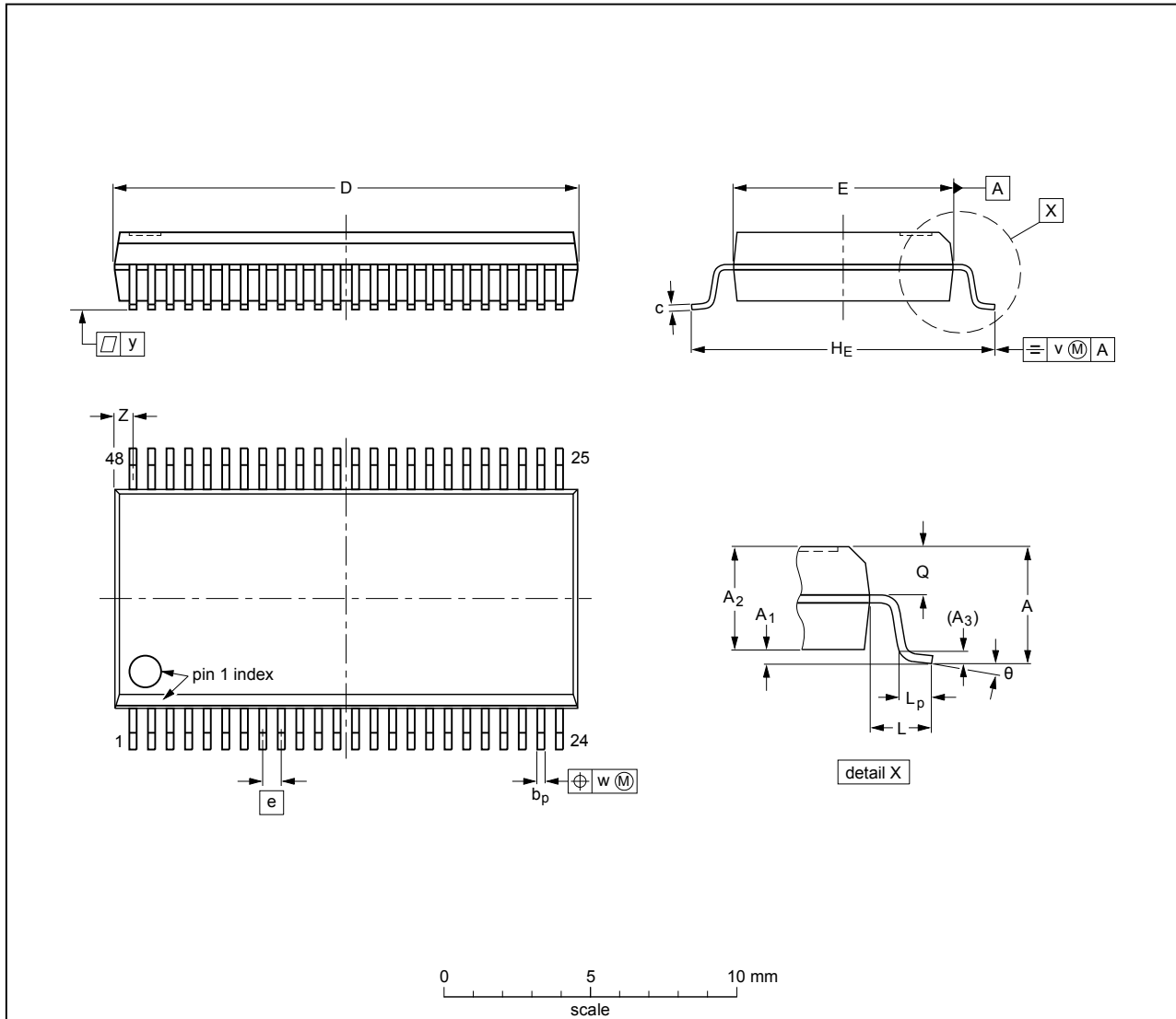
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

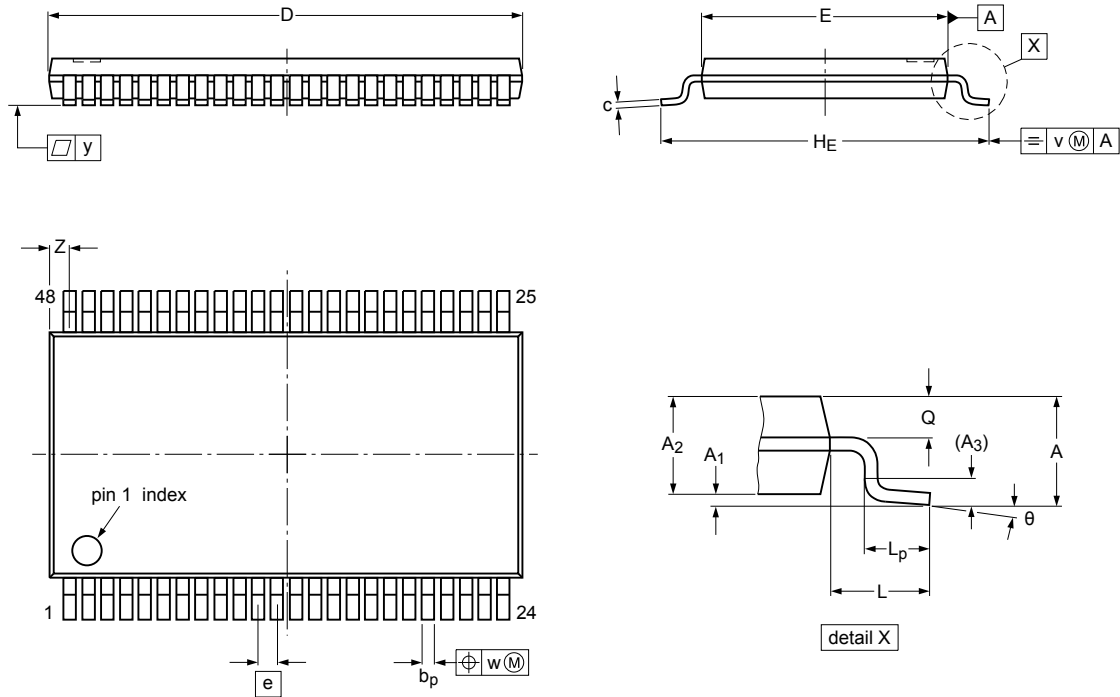
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

Fig. 8. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

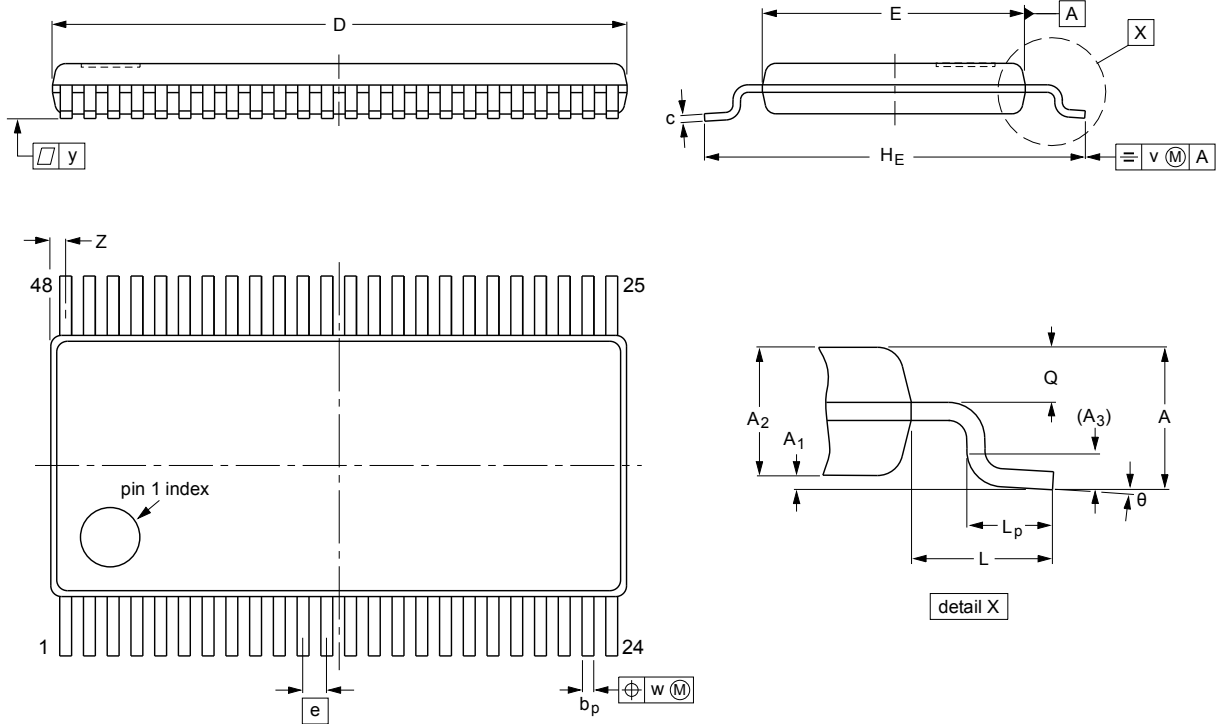
sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				-03-02-19- 13-08-05

Fig. 9. Package outline SOT362-1 (TSSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 4.4 mm; lead pitch 0.4 mm

SOT480-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.23 0.13	0.20 0.09	9.8 9.6	4.5 4.3	0.4	6.6 6.2	1	0.7 0.5	0.4 0.3	0.2	0.07	0.08	0.4 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT480-1		MO-153				99-12-27 03-02-18

Fig. 10. Package outline SOT480-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH16244A v.15	20190215	Product data sheet	-	74LVC_LVCH16244A v.14
Modifications:	<ul style="list-style-type: none"> Type numbers 74LVC16244AEV and 74LVCH16244AEV (SOT702-1) removed. Type numbers 74LVC16244ABX and 74LVCH16244ABX (SOT1134-2) removed. Type numbers 74LVC16244ADGV and 74LVCH16244ADGV (SOT480-1) added. 			
74LVC_LVCH16244A v.14	20170615	Product data sheet	-	74LVC_LVCH16244A v.13
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Fig. 1 updated. 			
74LVC_LVCH16244A v.13	20140207	Product data sheet	-	74LVC_LVCH16244A v.12
Modifications:	<ul style="list-style-type: none"> Table 5: Minimum V_{CC} changed from 2.3 V to 1.65 V (errata). 			
74LVC_LVCH16244A v.12	20120305	Product data sheet	-	74LVC_LVCH16244A v.11
74LVC_LVCH16244A v.11	20111027	Product data sheet	-	74LVC_LVCH16244A v.10
74LVC_LVCH16244A v.10	20110429	Product data sheet	-	74LVC_LVCH16244A v.9
74LVC_LVCH16244A v.9	20100318	Product data sheet	-	74LVC_LVCH16244A v.8
74LVC_LVCH16244A v.8	20081117	Product data sheet	-	74LVC_LVCH16244A v.7
74LVC_LVCH16244A v.7	20031208	Product specification	-	74LVC_LVCH16244A v.6
74LVC_LVCH16244A v.6	20030130	Product specification	-	74LVC_LVCH16244A v.5
74LVC_LVCH16244A v.5	20021030	Product specification	-	74LVC_H16244A v.4
74LVC_H16244A v.4	19971028	Product specification	-	74LVC16244A_74LVCH16244A v.3
74LVC16244A_74LVCH16244A v.3	19971028	Product specification	-	74LVC16244A v.2
74LVC16244A v.2	19970630	Product specification	-	74LVC16244A v.1
74LVC16244A v.1	-	-	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
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