

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHCV240FK TC74VHCV244FK

Octal Schmitt Bus Buffer

TC74VHCV240FK Inverted, 3-State Outputs
TC74VHCV244FK Non-Inverted, 3-State Outputs

The TC74VHCV240 and 244FK are advanced high speed CMOS OCTAL BUS BUFFERs fabricated with silicon gate CMOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The 74VHCV240FK is an inverting 3-state buffer having two active-low output enables. The TC74VHCV244FK is a non-inverting 3-state buffer, and has two active-low output enables.

Input pin have hysteresis between the positive-going and negative-going thresholds. Thus the TC74VHCV240 and 244FK are capable of squaring up transitions of slowly changing input signals and provides an improved noise immunity.



Weight VSSOP20-P-0030-0.50 : 0.03 g (typ.)

Input protection and output circuit ensure that 0 to 5.5 V can be applied to the input and output ^(Note) pins without regard to the supply voltage. These structure prevents device destruction due to mismatched supply and input/output voltages such as battery back up, etc.

Note: Output in off-state

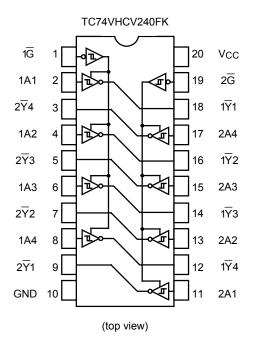
Features

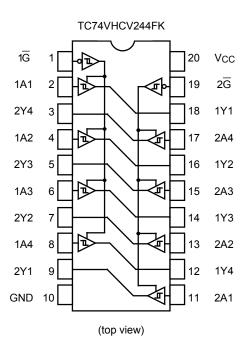
- High speed: tpd = 3.9 ns (typ.) at VCC = 5 V
- Low power dissipation: ICC = 2 μA (max) at Ta = 25°C
- Wide operating voltage range: VCC (opr) = 1.8 V to 5.5 V
- Ouput current: |IOH|/IOL = 16 mA (min) (VCC = 4.5 V)
- Available in VSSOP (US)
- Power-down protection provided on all inputs and outputs
- Pin and function compatible with the 74 series (74AC/VHC/HC/F/ALS/LS etc.) 240/244 type

Start of commercial production 2009-12



Pin Assignment





Truth Table

Inputs		Outputs				
ľG	An	Yn	\overline{Y}_{n}			
L	L	L	Н			
L	Н	Н	L			
Н	Х	Z	Z			

X: Don't care

Z: High impedance

Yn: TC74VHCV244FK

 \overline{Y}_n : TC74VHCV240FK



Absolute Maximum Ratings (Note1)

Characteristics	Symbol	Rating	Unit	
Supply voltage range	Vcc	−0.5 to 7.0	V	
DC input voltage	V _{IN}	-0.5 to 7.0	V	
DC output valtage	\/a	-0.5 to 7.0 (Note 2)	V	
DC output voltage	Vout	-0.5 to V _{CC} + 0.5 (Note 3)	v	
Input diode current	lıK	-50	mA	
Output diode current	lok	±50 (Note 4)	mA	
DC output current	lout	±50	mA	
Power dissipation	PD	180	mW	
DC V _{CC} /ground current	ICC/IGND	±100	mA	
Storage temperature	T _{stg}	−65 to 150	°C	

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: Output in off-state

Note 3: High or low state. IOUT absolute maximum rating must be observed.

Note 4: VOUT < GND, VOUT > VCC

Operating Ranges (Note1)

Characteristics	Symbol	Rating	Unit
Power supply voltage	Vcc	1.8 to 5.5	V
Input voltage	VIN	0 to 5.5	V
0 1 1	Vout	0 to 5.5 (Note 2)	V
Output voltage		0 to V _{CC} (Note 3)	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 20 (V _{CC} = 3.3 ± 0.3V) 0 to 1 (V _{CC} = 5 ± 0.5V)	ms/V

Note 1: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs must be tied to either VCC or GND.

Note 2: Output in off-state

Note 3: High or low state.



Electrical Characteristics

DC Characteristics

Characteristics	Test Condition		Ta = 25°C			Ta = −40 to 85°C		Unit		
				VCC (V)	Min	Тур.	Max	Min	Max	
		_		1.8	_	_	1.65	_	1.65	
				2.3	_	_	1.85	_	1.85	
Positive threshold voltage	VP			3.0	_	_	2.20	_	2.20	
				4.5	_	_	3.15	_	3.15	
				5.5	_	_	3.85	_	3.85	V
				1.8	0.15	_	_	0.15	_	v
				2.3	0.45	_	_	0.45	_	
Negative threshold voltage	VN	_		3.0	0.90	_	_	0.90	_	
				4.5	1.35	_	_	1.35	_	
				5.5	1.65	_	_	1.65	_	
				1.8	0.15	_	1.05	0.15	1.05	
		_		2.3	0.20	_	1.10	0.20	1.10	V
Hysteresis voltage	VH			3.0	0.30	_	1.20	0.30	1.20	
				4.5	0.40	_	1.40	0.40	1.40	
				5.5	0.50	_	1.60	0.50	1.60	
	Vон	VIN = VIH or VIL	I _{OH} = -50 μA	1.8	1.7	1.8	_	1.7	_	-
				3.0	2.9	3.0	_	2.9	_	
High-level output voltage				4.5	4.4	4.5	_	4.4	_	
			$I_{OH} = -8 \text{ mA}$	3.0	2.58		_	2.48	_	
			I _{OH} = −16 mA	4.5	3.94	_	_	3.80	_	
	I VOI I			1.8		0.0	0.1	-	0.1	V
			I _{OL} = 50 μA	3.0	_	0.0	0.1	_	0.1	
Low-level output voltage		VIN	·	4.5	_	0.0	0.1	_	0.1	
		= VIH or VIL	I _{OL} = 8 mA	3.0	_	_	0.36		0.44	
			I _{OL} = 16 mA	4.5	_	_	0.44	_	0.55	
3-state output off-state current	loz	V _{IN} = V _{IH} or V _{IL} V _{OUT} = 0 to 5.5V		1.8 to 5.5	_	_	±0.5	_	±5.0	μА
Power-off leakage current	loff	V _{IN} /V _{OUT} = 5.5 V		0	_	_	0.5	_	5.0	μА
Input leakage current	I _{IN}	V _{IN} = 5.5 V or GND		0 to 5.5		_	±0.1	_	±1.0	μА
Quiescent supply current	Icc	VIN = VCC or	GND	5.5	_	_	2.0	_	20.0	μА



AC Characteristics (input: tr = tf = 3 ns)

Characteristics Symbol		Tes	st Condition		Ta = 25°C			Ta = -40 to 85°C		Unit
-,		V _{CC} (V)	C _L (pF)	Min	Тур.	Max	Min	Max	Onne	
		_	2.5 ± 0.2	15	_	6.4	11.6	1.0	14.0	
				50	_	9.2	14.4	1.0	17.0	
Propagation delay time	t_{pLH}			15	_	5.0	7.5	1.0	9.0	
(TC74VHCV240)	t _{pHL}		3.3 ± 0.3	50	_	7.0	11.0	1.0	12.5	ns
			E 0 + 0 E	15	_	3.9	5.5	1.0	6.5	
			5.0 ± 0.5	50	_	5.4	7.5	1.0	8.5	
			2.5 ± 0.2	15	_	6.7	12.5	1.0	15.0	
			2.5 ± 0.2	50	_	9.5	15.3	1.0	18.0	
Propagation delay time	t _{pLH}		22 02	15	_	5.0	8.4	1.0	10.0	20
(TC74VHCV244)	t _{pHL}	_	3.3 ± 0.3	50	_	7.2	11.9	1.0	13.5	ns
			50.05	15	_	3.8	5.5	1.0	6.5	
			5.0 ± 0.5	50	_	5.4	7.5	1.0	8.5	
	t _P ZL t _P ZH	$R_L = 1 \text{ k}\Omega$	2.5 ± 0.2	15	_	7.8	14.6	1.0	17.0	ns
				50	_	11.1	17.8	1.0	21.0	
3-state output enable			3.3 ± 0.3	15	_	5.7	10.6	1.0	12.5	
time				50	_	8.4	14.1	1.0	16.0	
			5.0 ± 0.5	15	_	4.1	7.3	1.0	8.5	
				50	_	6.2	9.3	1.0	10.5	
			2.5 ± 0.2	50	_	14.3	19.2	1.0	21.0	
3-state output disable time	t _{pLZ} t _{pHZ}	$R_L = 1 k\Omega$	3.3 ± 0.3	50	_	10.9	14.0	1.0	16.0	ns
tpH.	νрн∠		5.0 ± 0.5	50	_	8.7	9.2	1.0	10.5	
			2.5 ± 0.2	50	_	_	2.0	-	2.0	
Output to output skew	t _{osLH} t _{osHL}	(Note 1)	3.3 ± 0.3	50	_	_	1.5	-	1.5	ns
	USHL		5.0 ± 0.5	50	_	_	1.0	_	1.0	
Input capacitance	C _{IN}		_		_	4	10	_	10	pF
Output capacitance	Cout		_		_	6	_	_	_	pF
Power dissipation	0	TC74VHCV240		_	20	_	_	_		
capacitance (Note 2)	C _{PD}	TC74VHCV24	TC74VHCV244		_	21	_	_	_	- pF

Note 1: Parameter guaranteed by design.

 $tosLH = |tpLHm - tpLHn|, \ tosHL = |tpHLm - tpHLn|$

Note 2: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

ICC (opr) = $CPD \cdot VCC \cdot fIN + ICC / 8$ (per bit)



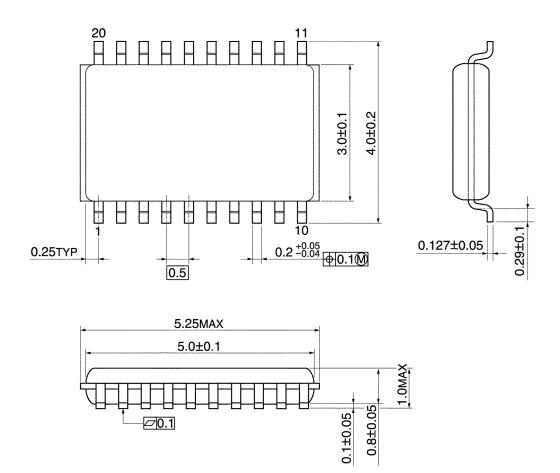
Noise Characteristics (input: tr = tf = 3 ns)

Characteristics	Cymhol	Test Condition		Ta =	Ta = 25°C	
Characteristics	Symbol		V _{CC} (V)	Тур.	Limit	Unit
Quiet output maximum dynamic VoL	VOLP	0. 505	3.3	0.45	_	V
Quiet output maximum dynamic VOL		C _L = 50 pF	5.0	0.9	_	
Quiet output minimum dynamic VOL	Volv	C _L = 50 pF	3.3	-0.1	-	V
Quiet output minimum dynamic VOL			5.0	-0.3	1	
Minimum high level dynamic input voltage	V_{IHD}	C _L = 50 pF	5.0	_	3.5	V
Maximum low level dynamic input voltage	VILD	C _L = 50 pF	5.0	_	1.5	V



Package Dimensions

VSSOP20-P-0030-0.50 Unit: mm



Weight: 0.03 g (typ.)



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