TPS6305x Single Inductor Buck-Boost With 1-A Switches and Adjustable Soft Start

1 Features

- Real Buck or Boost with Seamless Transition Between Buck and Boost Mode
- 2.5 V to 5.5 V Input Voltage Range
- 0.5-A Continuous Output Current: V_{IN} ≥ 2.5 V, V_{OUT} = 3.3 V
- Adjustable and Fixed Output Voltage Version
- Efficiency > 90% in Boost Mode and > 95% in Buck Mode
- 2.5-MHz Typical Switching Frequency
- Adjustable Average Input Current Limit
- Adjustable Soft-Start Time
- Device Quiescent Current < 60 µA
- Automatic Power Save Mode or Forced PWM Mode
- Load Disconnect During Shutdown
- Overtemperature Protection
- Small 1.6mm x 1.2mm, 12-pin WCSP and 2.5mm x 2.5mm 12-pin HotRod™ QFN package

2 Applications

- Cellular and Smart Phones
- Tablets PC
- PC and Smart Phone Accessories
- Battery Powered Applications
- Smart Grid/Smart Meter

3 Description

The TPS6305x family of devices is a high efficiency, low quiescent-current buck-boost converter, suitable for applications where the input voltage is higher or lower than the output.

Continuous output current can go as high as 500 mA in boost mode and as high as 1 A in buck mode. The maximum average current in the switches is limited to a typical value of 1 A. The TPS6305x family of devices regulate the output voltage over the complete input voltage range by automatically switching between buck or boost mode depending on the input voltage, ensuring seamless transition between modes.

The buck-boost converter is based on a fixed-frequency, pulse-width-modulation (PWM) controller using synchronous rectification to obtain the highest efficiency. At low load currents, the converter enters Power Save Mode to maintain high efficiency over the complete load current range.

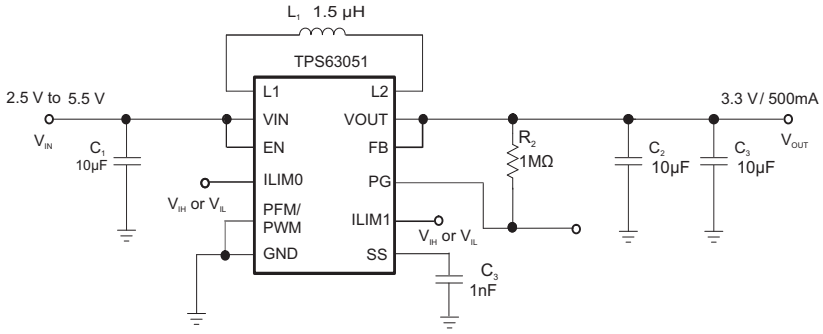
The PFM/PWM pin allows the user to select between automatic-PFM/PWM mode operation and forced-PWM operation. During PWM mode a fixed-frequency of typically 2.5 MHz is used. The output voltage is programmable using an external resistor divider, or is fixed internally on the chip. The converter can be disabled to minimize battery drain. During shutdown, the load is disconnected from the battery. The device is packaged in a 12-pin DSBGA and in a 12-pin HotRod package.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS63050	DSBGA (12)	1.56mm x 1.16mm
TPS63051	VQFN (12)	2.50mm × 2.50mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic (WCSP)



Efficiency vs Output Current

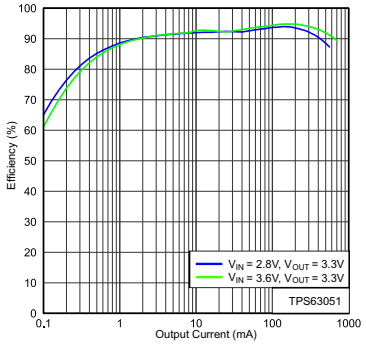


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2015) to Revision C — **Page**

- Added new package option to Features ... 1
- Added VQFN package to Device Information table ... 1
- Added HotRod Pin Configuration and Functions ... 3
- Added Parameter Measurement Circuit for HotRod package option ... 14

Changes from Revision A (February 2014) to Revision B — **Page**

- Changed Description section ... 1
- Changed graphic image ... 1
- Changed "Ordering Information" table to "Device Comparison Table" ... 3
- Changed "Handling Ratings" table to "ESD Rating" table and moved T_{stg} spec to the Absolute Maximum Ratings table ... 4
- Moved some Typical Characteristics graphs to the Application Curves section ... 7

Changes from Original (July 2013) to Revision A — **Page**

- Added *Device Information* and *ESD Rating* tables, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Added TPS63050 device specifications and description throughout data sheet ... 1
- Changed , PCB Layout ... 21
- Changed , PCB Layout ... 21

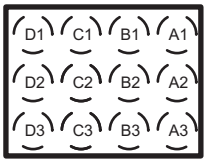
5 Device Comparison Table

PART NUMBER (1)	V_{OUT}
TPS63050	Adjustable
TPS63051	3.3 V

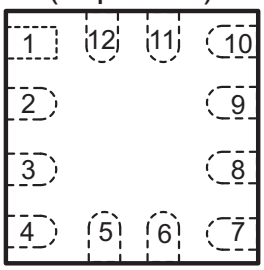
(1) For all available packages, see the orderable addendum at the end of the datasheet

6 Pin Configuration and Functions

YFF Package
12-Pin DSBGA
(TOP VIEW)



RMW Package
12-Pin HotRod
(Top View)



Pin Functions

TERMINAL			I/O	DESCRIPTION
NAME	WCSP	HotRod		
EN	A3	11	I	Enable input. (1 enabled, 0 disabled). It must not be left floating
FB	D2	5	I	Voltage feedback of adjustable versions, must be connected to VOUT on fixed output voltage versions1
GND	B1	2,9		Ground for Power stage and Control stage
ILIM0	B2	10	I	Programmable inrush current limit input works together with I_{LIM1}. See table on page 1. It must not be left floating
ILIM1	B3	See (1)	I	Programmable inrush current limit input works together with I_{LIM0}. See Efficiency vs Output Current on page 1. Do not leave floating
L1	A1	1		Connection for Inductor
L2	C1	3		Connection for Inductor
PFM/PWM	C2	6	I	0 for PFM mode 1 for forced PWM mode. It must not be left floating
PG	C3	8	O	Power good open drain output
SS	D3	7	I	Adjustable Soft-Start. If left floating default soft-start time is set
VIN	A2	12	I	Supply voltage for power stage and control stage
VOUT	D1	4	O	Buck-boost converter output

(1) Only available with DSBGA package, for VQFN package ILIM1 is internally connected to voltage level > V_{IH}

7 Specifications

7.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage(2)	V_{IN}, L1, EN, V_{OUT}, FB, V_{IN}A, PFM/PWM	–0.3	7	V
	L2(3)	–0.3	7	
	L2(4)	–0.3	9.5	
Operating junction temperature, T_J		–40	150	°C
Operating ambient temperature, T_A		–40	85	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.
(3) DC voltage rating.
(4) AC voltage rating.

7.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±700	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

See (1)		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2.5		5.5	V
I_{OUT}	Output current			0.5	A
L	Inductance(2)	1	1.5	2.2	µH
C_{OUT}	Output capacitance(3)	10			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating virtual junction temperature	–40		125	°C

(1) Refer to the Application Information section for further information
(2) Effective inductance value at operating condition. The nominal value given matches a typical inductor to be chosen to meet the inductance required.
(3) Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower then the nominal value when a voltage is applied. This is why the capacitance is specified to allow the selection of the nominal capacitor required with the DC bias effect for this type of capacitor. The nominal value given matches a typical capacitor to be chosen to meet the minimum capacitance required.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6305x		UNIT
		WCSP	RMW	
		12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	89.9	37.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.7	30.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.9	8.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.9	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.7	7.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	2.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 3.6 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY							
V_{IN}	Input voltage range			2.5		5.5	V
V_{IN_Min}	Minimum input voltage to turn on in full load		I_{OUT} = 500 mA		2.7		V
I_{OUT}	Output current(1)		I_{LIM0} = V_{IH}, I_{LIM1} = V_{IH},		500		mA
I_Q	Quiescent current	V_{IN}	I_{OUT} = 0 mA, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V		43	60	µA
		V_{OUT}	I_{OUT} = 0 mA, EN = V_{IN} = 3.6 V, V_{OUT} = 3.3 V			10	
I_{sd}	Shutdown current		EN = 0 V		0.1	1	µA
$UVLO_{TH}$	Undervoltage lockout threshold		V_{IN} falling	1.6	1.7	1.8	V
$UVLO_{hys}$	Undervoltage lockout hysteresis				200		mV
T_{SD}	Thermal shutdown		Temperature rising		140		°C
T_{SD}(hys)	Thermal shutdown hysteresis				20		°C
LOGIC SIGNALS EN, I_{LIM0}, I_{LIM1}							
V_{IH}	High level input voltage		V_{IN} = 2.5 V to 5.5 V	1.2			V
V_{IL}	Low level voltage Input Voltage		V_{IN} = 2.5 V to 5.5 V			0.3	V
I_{lkg}	Input leakage current		PFM / PWM, EN, I_{LIM0}, I_{LIM1} = GND or V_{IN}		0.01	0.1	µA
POWER GOOD							
V_{OL}	Low level voltage		I_{sink} = 100 µA			0.3	V
I_{PG}	PG sinking current		V = 0.3 V			0.1	mA
I_{lkg}	Input leakage current		V_{PG} = 3.6 V		0.01	0.1	µA
OUTPUT							
V_{OUT}	Output voltage range			2.5		5.5	V
V_{FB}	TPS63050 feedback regulation voltage				0.8		V
V_{FB}	TPS63050 feedback voltage accuracy		PWM mode	–1.1%		1.1%	
V_{FB}	TPS63050 feedback voltage accuracy(2)		PFM mode	–1%		3%	
V_{OUT}	TPS63051 output voltage accuracy		PWM mode	3.27	3.3	3.34	V
V_{OUT}	TPS63051 output voltage accuracy(2)		PFM mode	3.27	3.3	3.39	V
$I_{PWM->PFM}$	Minimum output current to enter PFM mode		V_{IN} = 3 V; V_{OUT} = 3.3 V		150		mA
I_{FB}	TPS63050 feedback input bias current		V_{FB} = 0.8 V		10	100	nA
$R_{DS(on)}$	Input high-side FET on-resistance		I_{SW} = 500 mA		145		mΩ
	Output high-side FET on-resistance		I_{SW} = 500 mA		95		mΩ
	Input low-side FET on-resistance		I_{SW} = 500 mA		170		mΩ
	Output low-side FET on-resistance		I_{SW} = 500 mA		115		mΩ
I_{IN_MAX}	Input current-limit boost mode		I_{LIM0} = V_{IH}, I_{LIM1} = V_{IH},V_{IN} = 2.7 V to 3 V, V_{OUT} = 3 V	480		1240	mA
			I_{LIM0} = V_{IH}, I_{LIM1} = V_{IH},V_{IN} = 2.7 V to 3.3 V, V_{OUT} = 3.3 V,	550		1400	mA
			I_{LIM0} = V_{IH}, I_{LIM1} = V_{IH},V_{IN} = 2.7 V to 4.5 V, V_{OUT} = 4.5 V,	630		1950	mA

(1) For minimum and maximum output current in a specific working point see Figure 1 and Figure 2; and Equation 1 through Equation 4.
(2) Conditions: f = 2.5 MHz, L = 1.5 µH, C_{OUT} = 10 µF

Electrical Characteristics (continued)

V_{IN} = 3.6 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SS_IN}	Programmable inrush current limit(3)	I_{LIM0} = V_{IL}, I_{LIM1} = V_{IL}, V_{IN} = 3.0 V,V_{OUT} = 3.3 V, (Available for DBGA only)		0.4×I_{IN_MAX}		mA
		I_{LIM0} = V_{IH}, I_{LIM1} = V_{IL}, V_{IN} = 3.0 V,V_{OUT} = 3.3 V, (Available for DBGA only)		0.5×I_{IN_MAX}		
		I_{LIM0} = V_{IL}, I_{LIM1} = V_{IH}, V_{IN} = 3.0 V,V_{OUT} = 3.3 V		0.65×I_{IN_MAX}		
		I_{LIM0} = V_{IH}, I_{LIM1} = V_{IH}, V_{IN} = 3.0 V,V_{OUT} = 3.3 V		I_{IN_MAX}		
I_{SS}	Soft-start current TPS63051			1		µA
I_{SS}	Soft-start current TPS63050			3.2		µA
	Line regulation	V_{IN} = 2.5 V to 5.5 V, I_{OUT} = 500 mA, PWM mode		0.963		mV/V
	Load regulation	V_{IN} = 3.6 V, I_{OUT} = 0 mA to 500 mA, PWM mode		4		mV/A

(3) For variation of this parameter with Input voltage see Figure 3.

7.6 Switching Characteristics

V_{IN} = 3.6 V, T_J = –40°C to 125°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT						
f_s	Switching frequency			2.5		MHz
t_{SS}	Softstart time	V_{OUT} = EN = low to high, SS = floating, Buck mode V_{IN} = 3.6 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA(1)		280		µs
		V_{OUT} = EN = low to high, SS = floating, Boost mode V_{IN} = 2.5 V, V_{OUT} = 3.3 V, I_{OUT} = 500 mA(1)		600		
t_d	Start up delay	Time from when EN = high to when device starts switching		100		µs

(1) For variation of this parameter with Input voltage see Figure 3.

7.7 Typical Characteristics

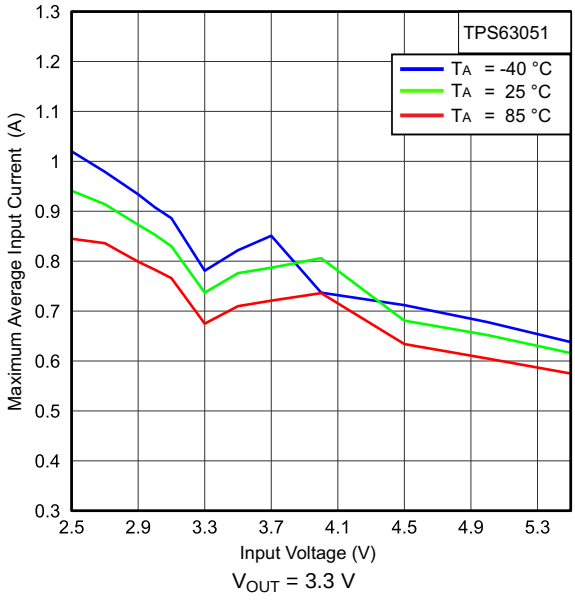


Figure 1. Maximum Average Input Current vs Input Voltage

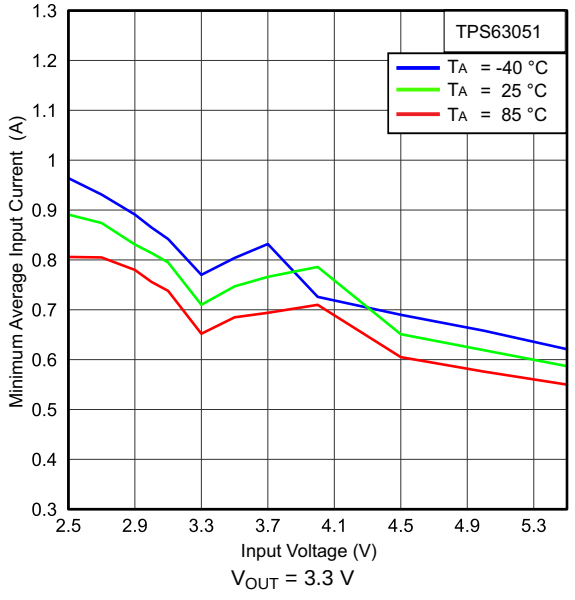


Figure 2. Minimum Average Input Current vs Input Voltage

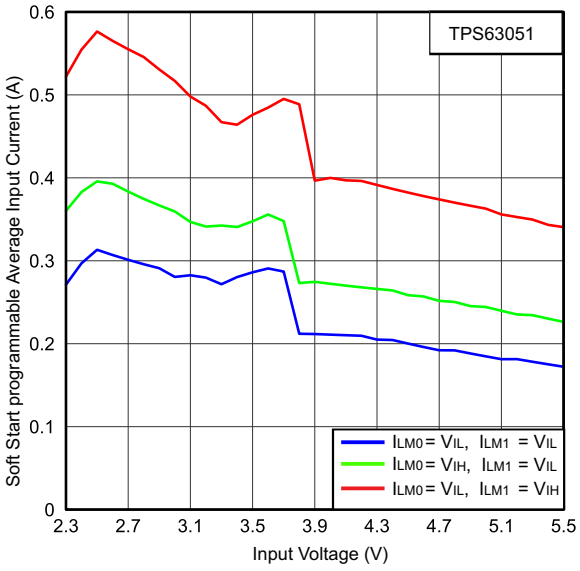


Figure 3. Programmable Average Input Current vs Input Voltage(1)

(1) All options only available with the DSBGA package. For VQFN package ILIM1 is internally connected to voltage level > V_{IH}

8 Detailed Description

8.1 Overview

The TPS6305x devices use 4 internal N-channel MOSFETs to maintain synchronous power conversion at all possible operating conditions. This enables the device to keep high efficiency over the complete input voltage and output power range. To regulate the output voltage at all possible input voltage conditions, the device automatically switches from buck operation to boost operation and back as required by the configuration. It always uses one active switch, one rectifying switch, one switch held on, and one switch held off. Therefore, it operates as a buck converter when the input voltage is higher than the output voltage, and as a boost converter when the input voltage is lower than the output voltage. There is no mode of operation in which all 4 switches are switching at the same time. Keeping one switch on and one switch off eliminates their switching losses. The RMS current through the switches and the inductor is kept at a minimum, to minimize switching and conduction losses. Controlling the switches this way allows the converter to always keep higher efficiency.

The device provides a seamless transition from buck to boost or from boost to buck operation.

8.2 Functional Block Diagrams

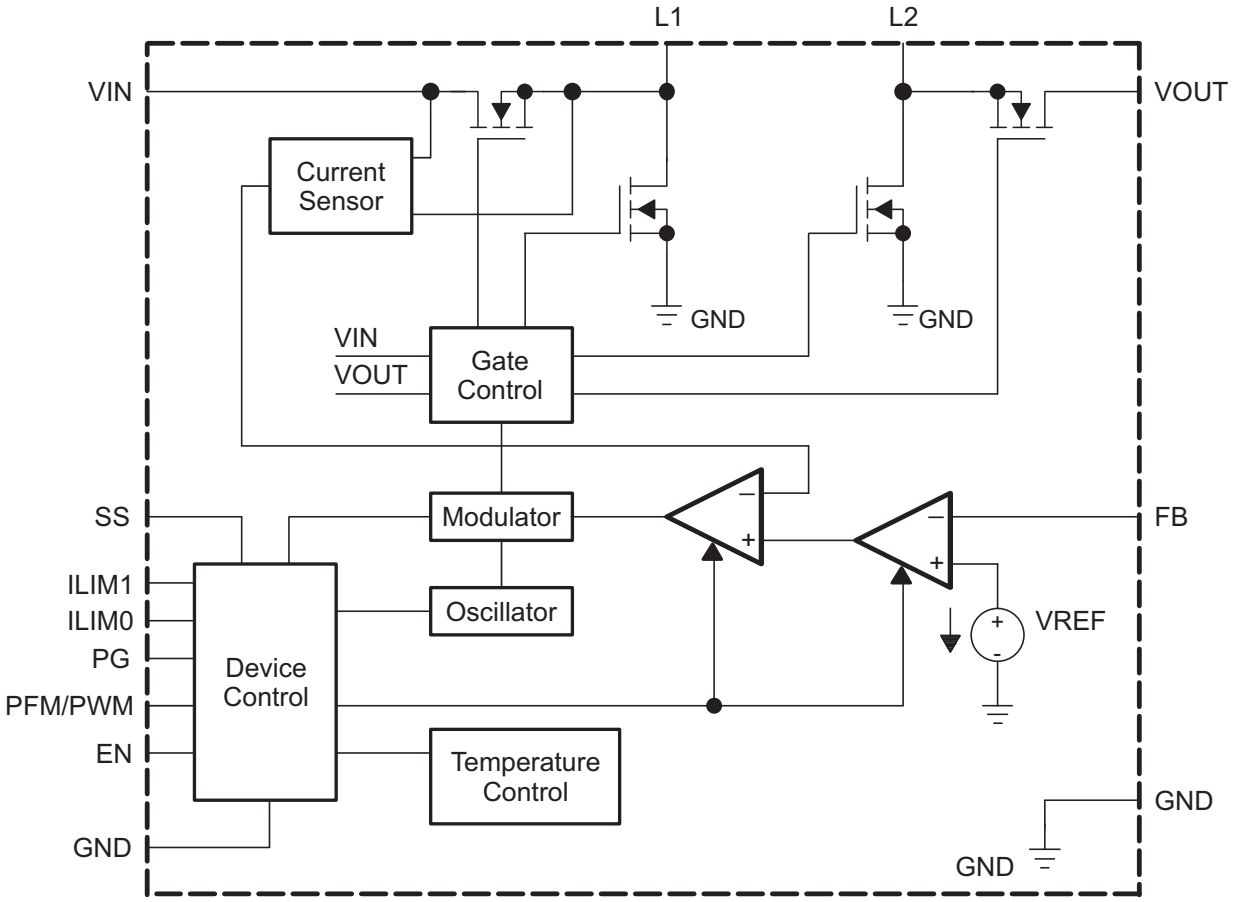


Figure 4. TPS63050 Block Diagram

Functional Block Diagrams (continued)

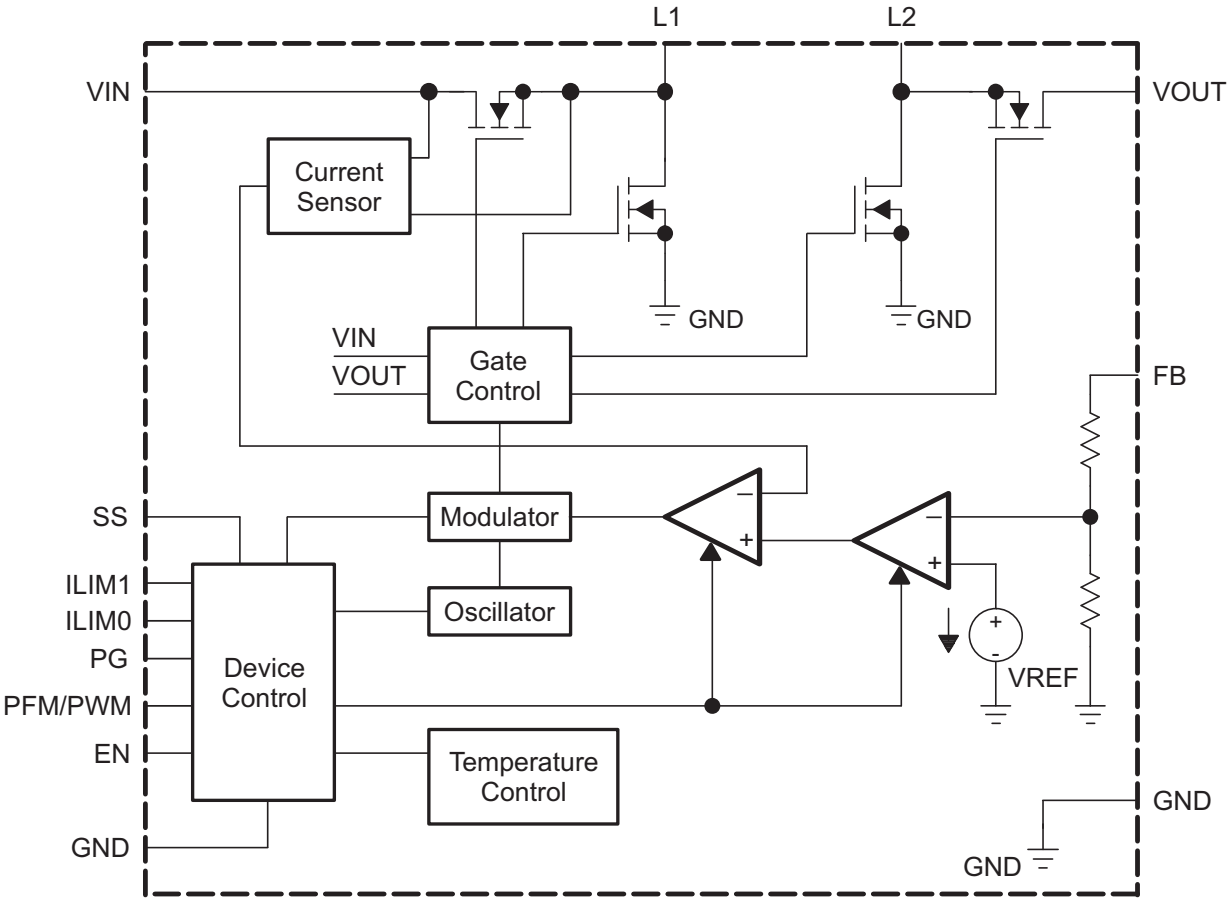


Figure 5. TPS63051 Block Diagram

8.3 Feature Description

8.3.1 Power Good

The TPS6305x devices have a PG output. The power good goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 0.1 mA. The power good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The power good is valid as long as the converter is enabled and V_{IN} is present. The power good goes low when the device is in undervoltage lockout, in thermal shutdown or in current limit.

If EN is pulled low and one of the pins I_{LIM0} or I_{LIM1} is high, then the PG pin is low. If both pins, I_{LIM0} and I_{LIM1} are low, the PG is open drain. In this case the PG pin, follows its pullup voltage. If this is not desired, one of the two pins I_{LIM0} or I_{LIM1}, must be set high. Table 1 lists the PG pin functionality.

Table 1. Power Good Settings

EN	ILIM1	ILIM0	PG
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	Open Drain

8.3.2 Overvoltage Protection

Overvoltage protection is implemented to limit the maximum output voltage. In case of overvoltage condition, the voltage amplifier regulates the output voltage to typically 6.7 V.

8.3.3 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 1.7 V with a 200-mV hysteresis.

8.3.4 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 140°C with a 20°C hysteresis.

8.3.5 Soft Start

To minimize inrush current and output voltage overshoot during start up, the device has a soft start. At turn on, the input current raises monotonically until the output voltage reaches regulation. The TPS6305x devices charge the soft start capacitor, at the SS pin, with a constant current of typically 1 µA. The input current follows the current used to charge the capacitor at the SS pin. The soft start operation is completed once the voltage at the SS pin has reached typically 1.3 V. Figure 3 shows the value of the soft start capacitor in respect to the soft-start time.

The soft-start time is the time from when the EN pin is asserted to when the output voltage has reached 90% of its nominal value. There is typically a 100-µs delay time from EN pin assertion to the start of the switching activity. The soft-start time depends on the load current, the input voltage, and the output capacitor. The soft-start time in boost mode is longer then the time in buck mode and it also depends on the load current, input voltage and output capacitor.

The soft-start time in Figure 3 is referred to typical application with 10-µF effective output capacitance.

The inductor current is able to increase and always assure a soft start unless a real short circuit is applied at the output.

8.3.6 Short Circuit Protection

The TPS6305x devices provide short circuit protection. When the output voltage does not increase above 1.2 V, a short circuit is detected and the output current is limited to 1.5 A.

8.4 Device Functional Modes

8.4.1 Control Loop Description

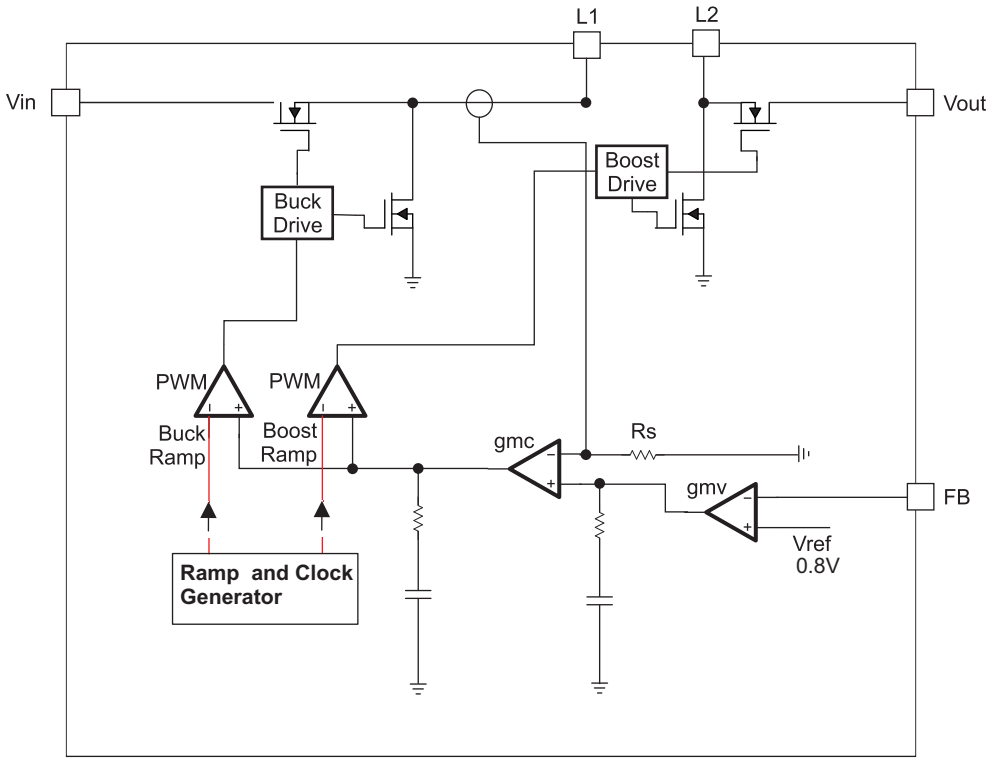


Figure 6. Average Current Mode Control

The controller circuit of the device is based on an average current mode topology. The average inductor current is regulated by a fast current regulator loop which is controlled by a voltage control loop. Figure 6 shows the control loop.

The noninverting input of the transconductance amplifier, gm_v, is assumed to be constant. The output of gm_v defines the average inductor current. The inductor current is reconstructed by measuring the current through the high side buck MOSFET. This current corresponds exactly to the inductor current in boost mode. In buck mode the current is measured during the on time of the same MOSFET. During the off time, the current is reconstructed internally starting from the peak value at the end of the on time cycle. The average current and the feedback from the error amplifier gm_v forms the correction signal gm_c. This correction signal is compared to the buck and the boost sawtooth ramp giving the PWM signal. Depending on which of the two ramps the gm_c output crosses either the Buck or the Boost stage is initiated. When the input voltage is close to the output voltage, one buck cycle is always followed by a boost cycle. In this condition, no more than three cycles in a row of the same mode are allowed. This control method in the buck-boost region ensures a robust control and the highest efficiency.

Device Functional Modes (continued)

8.4.2 Power Save Mode Operation

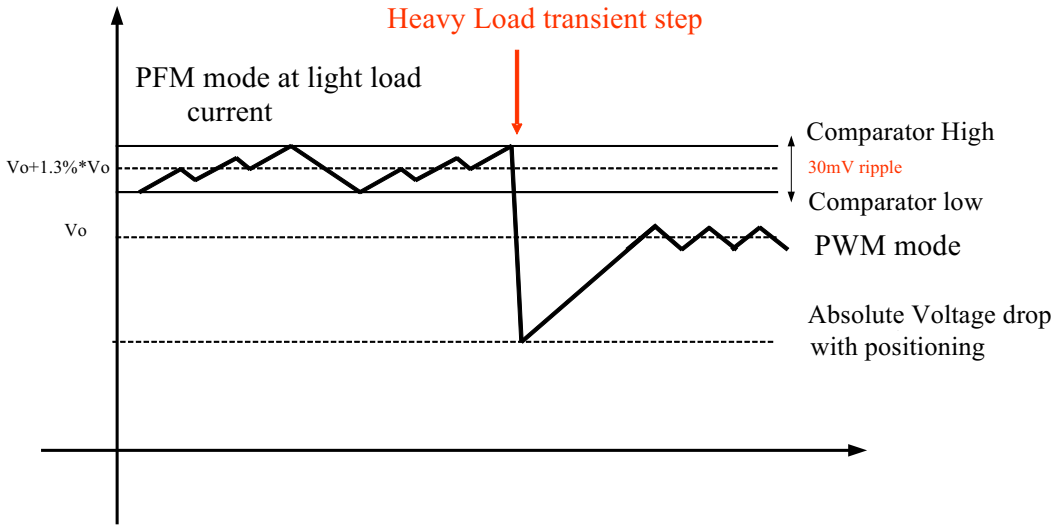


Figure 7. Power Save Mode Operation

Depending on the load current, the device works in PWM mode at load currents of approximately 350 mA or higher to provide the best efficiency over the complete load range. At lighter loads, the device switches automatically into Power Save Mode to reduce power consumption and extend battery life. The PFM/PWM pin is used to select between the two different operation modes. To enable Power Save Mode, the PFM/PWM pin must be set low.

During Power Save Mode, the part operates with a reduced switching frequency and lowest supply current to maintain high efficiency. The output voltage is monitored with a comparator at every clock cycle by the thresholds comp low and comp high. When the device enters Power Save Mode, the converter stops operating and the output voltage drops. The slope of the output voltage depends on the load and the output capacitance. When the output voltage reaches the comp low threshold, at the next clock cycle the device ramps up the output voltage again, by starting operation. Operation can last for one or several pulses until the comp high threshold is reached. At the next clock cycle, if the load is still lower than 150 mA, the device switches off again and the same operation is repeated. If at the next clock cycle the load is above 150 mA, the device automatically switches to PWM mode.

To keep high efficiency in PFM mode, there is only one comparator active to keep the output voltage regulated. The AC ripple in this condition is increased, compared to the PWM mode. The amplitude of this voltage ripple in the worst case scenario is 50 mV peak to peak, (typically 30 mV peak to peak), with 10 µF of effective output capacitance. To avoid a critical voltage drop when switching from 0 A to full load, the output voltage in PFM mode is typically 1.5% above the nominal value in PWM mode. This is called Dynamic Voltage Positioning and allows the converter to operate with a small output capacitor and still have a low absolute voltage drop during heavy load transients.

Power Save Mode is disabled by setting the PFM/PWM pin high.

8.4.3 Adjustable Current Limit

The TPS6305x devices have an internal user programmable current limit that monitors the input current during start-up. This prevents high inrush current protecting the device and the application. During start-up the input current does not exceed the current limit that is set by I_{LIM0} pin and I_{LIM1} pin. Depending on the logic level applied at these two pins, switching between four different current limit-levels is possible. The variation of those values over input voltage and temperature is shown in Figure 1 through Figure 2. Adjusting the soft-start time further using the soft-start capacitor is possible.

I_{LIM0} and I_{LIM1} set the current limit as listed in Table 2.

Device Functional Modes (continued)

Table 2. Adjustable Current Limit

ILIM1	ILIM0	CURRENT LIMIT SET (WCSP)	CURRENT LIMIT SET (HotRod)
Low	Low	$0.4 \times I_{IN\_MAX}$	Not Available
Low	High	$0.5 \times I_{IN\_MAX}$	Not Available
High	Low	$0.65 \times I_{IN\_MAX}$	$0.65 \times I_{IN\_MAX}$
High	High	I_{IN_MAX}	I_{IN_MAX}

The I_{LIM0}, I_{LIM1} pins can be changed during operation.

Given the curves provided in Figure 1 through Figure 2, calculating the output current in the different condition in boost mode is possible using Equation 1 and Equation 2 and in buck mode using Equation 3 and Equation 4.

$$\text{Duty Cycle Boost} \quad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \tag{1}$$

$$\text{Output Current Boost} \quad I_{OUT} = \eta \times I_{IN} (1-D) \tag{2}$$

where

- η = Estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)
- I_{IN} = Minimum average input current (Figure 2 to Figure 2)

$$\text{Duty Cycle Buck} \quad D = \frac{V_{OUT}}{V_{IN}} \tag{3}$$

$$\text{Output Current Buck} \quad I_{OUT} = (\eta \times I_{IN}) / D \tag{4}$$

where

- For η, use the number from the efficiency curves or 0.9 as an assumption.

8.4.4 Device Enable

The device starts operation when the EN pin is set high. The device enters shutdown mode when the EN pin is set low. In shutdown mode, the regulator stops switching, all internal control circuitry is switched off, and the load is disconnected from the input.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers must validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6305x is a high efficiency, low quiescent current buck-boost converter suitable for applications where the input voltage is higher or lower than the output voltage. Continuous output current can go as high as 500 mA in boost mode and as high as 1 A in buck mode. The maximum average current in the switches is limited to a typical value of 1 A.

The efficiency measurements

9.2 Typical Application

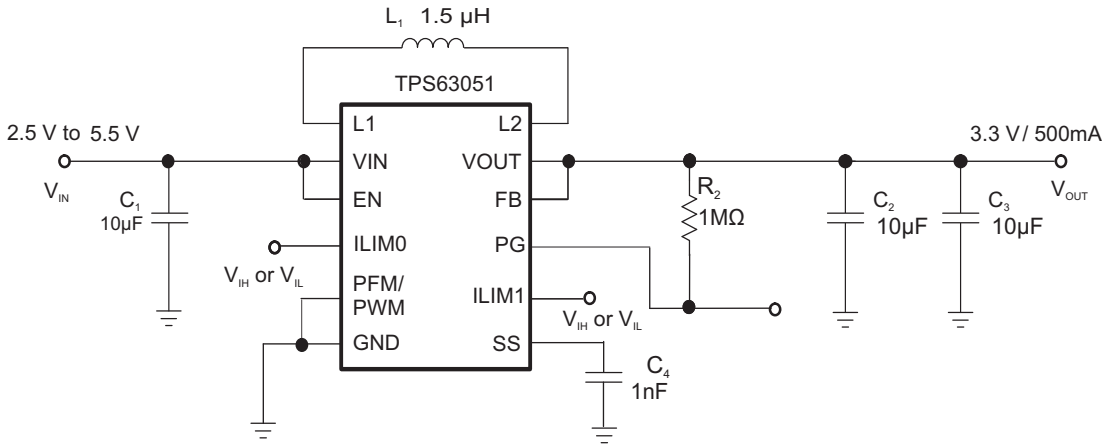


Figure 8. Parameter Measurement Circuit (WCSP)

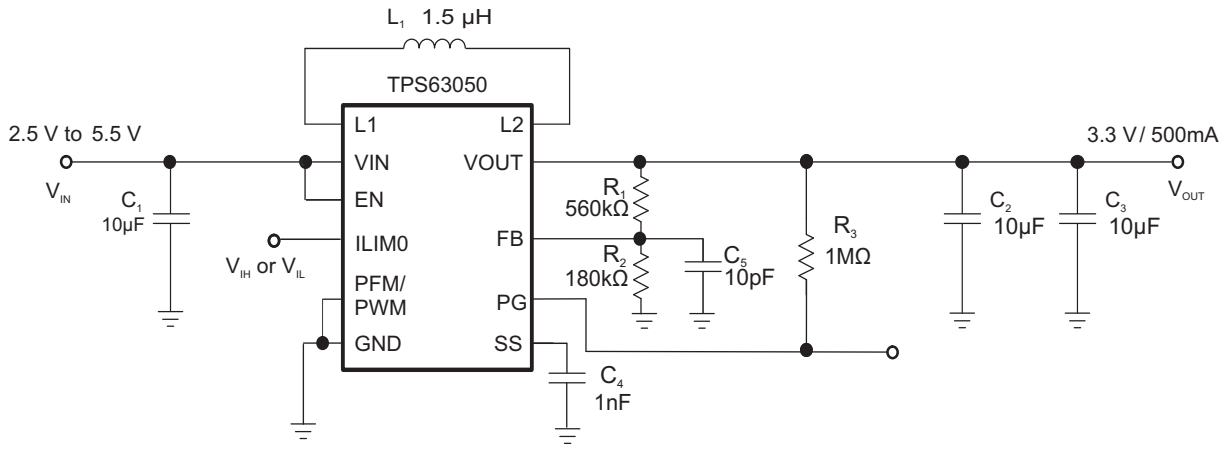


Figure 9. Parameter Measurement Circuit (HotRod)

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

Typical Application (continued)

9.2.2 Detailed Design Procedure

The first step is the selection of the output filter components, listed in Table 3. To simplify this process, Table 4 outlines possible inductor and capacitor value combinations.

Table 3. Components for Application Characteristic Curves

REFERENCE	DESCRIPTION	MANUFACTURER
	TPS6305x	Texas Instruments
L1	1.5 µH, 2.1 A, 108 mΩ	1269AS-H-1R5M, TOKO
C1, C2, C3	10 µF, 6.3 V, 0603, X5R ceramic	GRM188R60J106ME84D, Murata
C4	C_{SS}	
C5	10pF, only needed for the HotRod package version to filter ground noise when using external resistor divider	
R1	Depending on the output voltage of TPS6305x, 0 Ω with TPS63051	
R2	Depending on the output voltage of TPS6305x, not used withTPS63051	
R3	1 MΩ	

9.2.2.1 Output Filter Design

Table 4. Matrix of Output Capacitor and Inductor Combinations

NOMINAL INDUCTOR VALUE [µH](1)	NOMINAL OUTPUT CAPACITOR VALUE [µF](2)				
	10	20	44	66	100
1			+	+	+
1.5	+	+(3)	+	+	+
2.2			+	+	+

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by 20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by 20% and –50%.
(3) Typical application. Other check mark indicates recommended filter combinations

9.2.2.2 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into power save mode, and efficiency. See Table 5 for typical inductors.

Table 5. List of Recommended Inductors

INDUCTOR VALUE	COMPONENT SUPPLIER(1)	SIZE (L × W × H mm)	Isat / DCR
1 µH	TOKO 1286AS-H-1R0M	2 × 1.6 × 1.2	2.1 A / 68 mΩ
1.5 µH	TOKO, 1286AS-H-1R5M	2 × 1.6 × 1.2	2.5 A / 95 mΩ
1.5 µH	TOKO, 1269AS-H-1R5M	2.5 × 2 × 1	2.1 A / 90 mΩ
2.2 µH	TOKO 1286AS-H-2R2M	2 × 1.6 × 1.2	2 A / 160 mΩ

(1) See the *Third-Party Products Disclaimer* section.

For high efficiencies, the inductor must have a low dc resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 6. Only the equation which defines the switch current in boost mode is shown, because this provides the highest value of current and represents the critical current value for selecting inductor.

$$\text{Duty Cycle Boost} \qquad D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

where

- D = Duty Cycle in Boost mode

(5)

$$I_{PEAK} = \frac{Iout}{\eta \times (1 - D)} + \frac{Vin \times D}{2 \times f \times L}$$

where

- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an assumption)
  f = Converter switching frequency (typical 2.5MHz)
  L = Inductor value

(6)

NOTE

The calculation must be done for the minimum input voltage that is possible to have in boost mode.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It's recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 6. Possible inductors are listed in Table 5.

9.2.2.3 Capacitor selection

9.2.2.3.1 Input Capacitor

At least a 10-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended. This capacitance can be increased without limit.

9.2.2.3.2 Output Capacitor

Use of small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC, is recommended for the output capacitor. The recommended nominal output capacitance value is 10 µF with a variance as outlined in Table 4.

There is also no upper limit for the output capacitance value. Larger capacitors causes lower output voltage ripple as well as lower output voltage drop during load transients.

9.2.2.4 Setting the Output Voltage

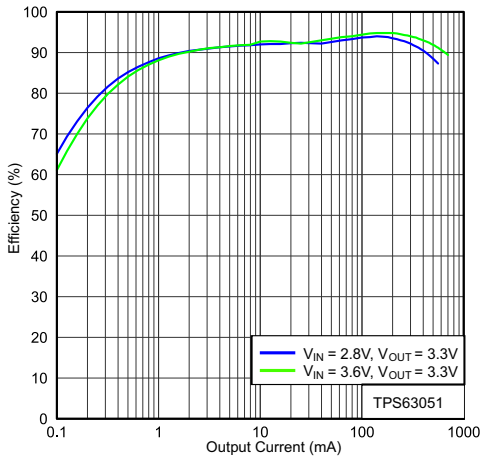
When the adjustable output voltage version TPS63050 is used, the output voltage is set by the external resistor divider. The resistor divider must be connected between VOUT, FB and GND. When the output voltage is regulated properly, the typical value of the voltage at the FB pin is 800 mV. The current through the resistive divider must be 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.1 µA, and the voltage across the resistor between FB and GND, R_2, is typically 800 mV. Based on these two values, the recommended value for R2 must be lower than 200 kΩ, in order to set the divider current at 3 µA or higher. It is recommended to keep the value for this resistor in the range of 200 kΩ. The value of the resistor connected between VOUT and FB, R1, depending on the needed output voltage (V_{OUT}), can be calculated using Equation 7:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

(7)

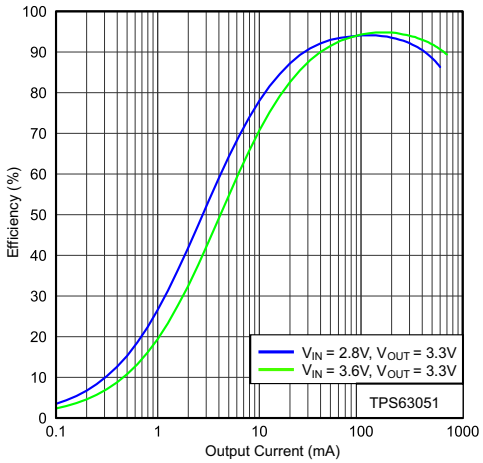
When using the HotRod package version of the TPS63050, it is recommended to add capacitor C_5, as shown in Figure 9. The capacitor on the feedback node is required to help filtering ground noise and matching the efficiency result shown in the Application Curves paragraph.

9.2.3 Application Curves



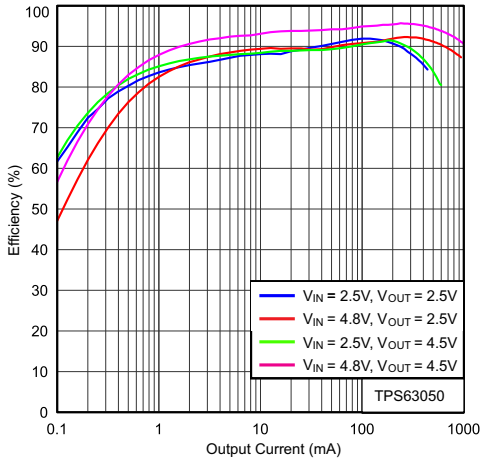
PFM/PWM = Low V_{OUT} = 3.3 V

Figure 10. Efficiency vs Output Current



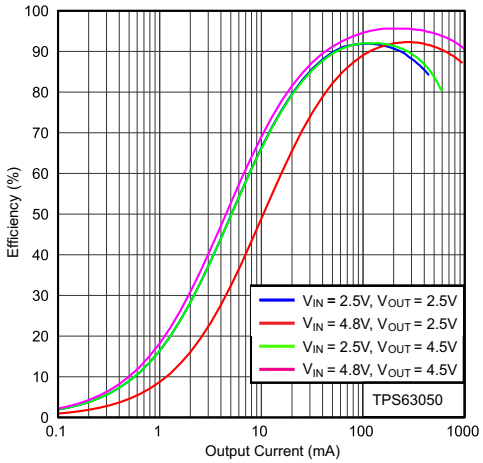
PFM/PWM = High V_{OUT} = 3.3 V

Figure 11. Efficiency vs Output Current



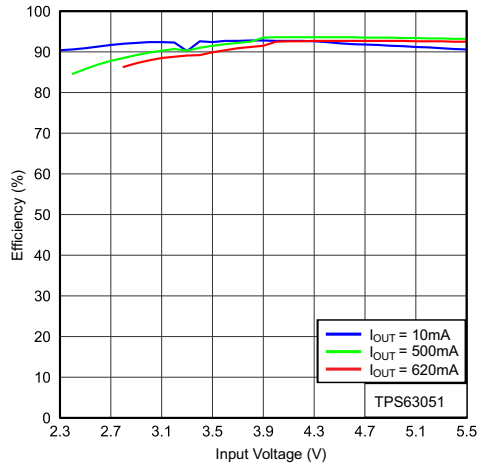
PFM/PWM = Low V_{OUT} = 2.5 V, 4.5 V

Figure 12. Efficiency vs Output Current



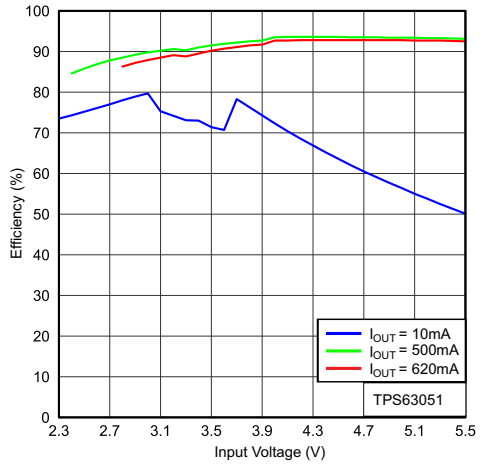
PFM/PWM = High V_{OUT} = 2.5 V, 4.5 V

Figure 13. Efficiency vs Output Current



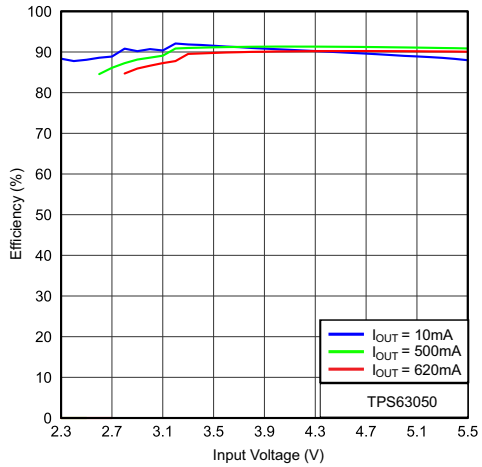
PFM/PWM = Low V_{OUT}= 3.3 V

Figure 14. Efficiency vs Input Voltage



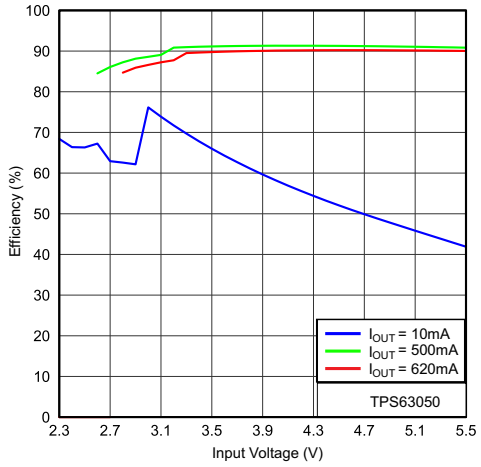
PFM/PWM = High V_{OUT}= 3.3 V

Figure 15. Efficiency vs Input Voltage



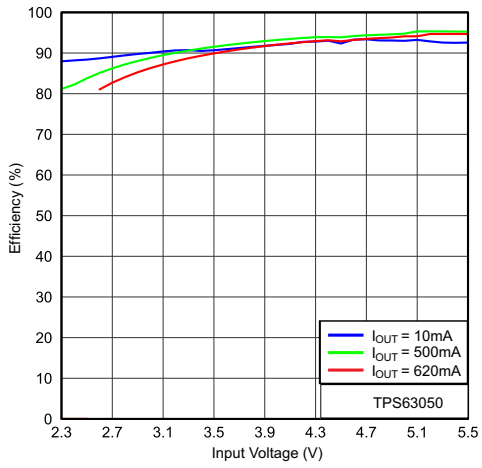
PFM/PWM = Low V_{OUT} = 2.5 V

Figure 16. Efficiency vs Input Voltage



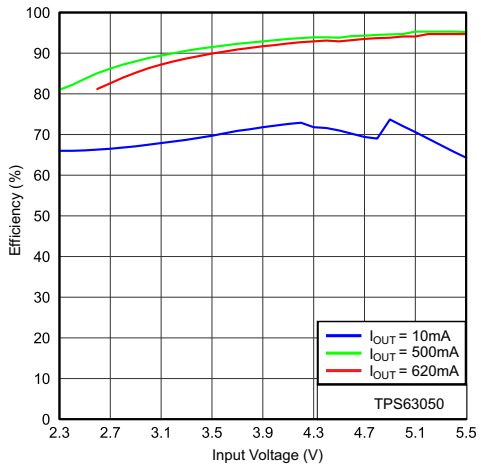
PFM/PWM = High V_{OUT} = 2.5 V

Figure 17. Efficiency vs Input Voltage



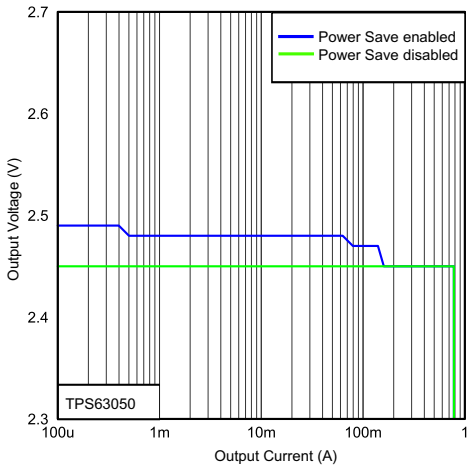
PFM/PWM = Low V_{OUT} = 4.5 V

Figure 18. Efficiency vs Input Voltage



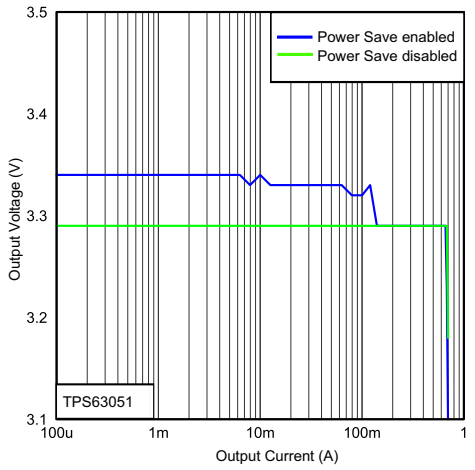
PFM/PWM =High V_{OUT}= 4.5 V

Figure 19. Efficiency vs Input Voltage



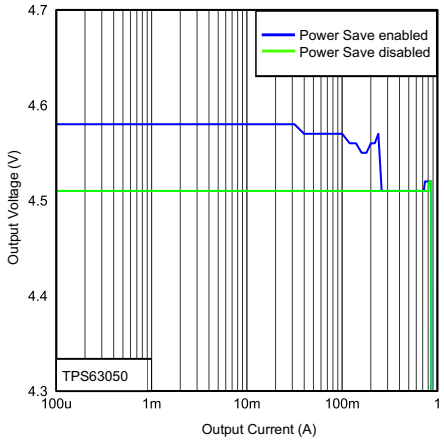
V_{IN} = 2.5 V

Figure 20. Output Voltage vs Output Current



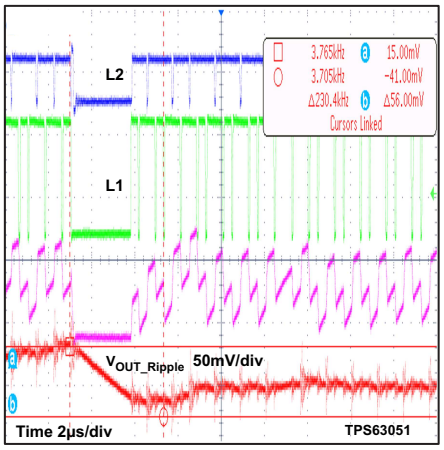
V_{IN} = 3.3 V

Figure 21. Output Voltage vs Output Current



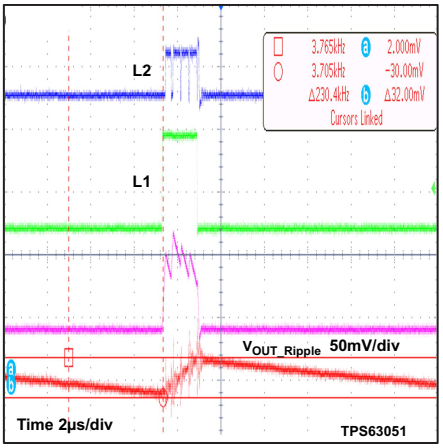
V_{IN} = 4.5 V

Figure 22. Output Voltage vs Output Current



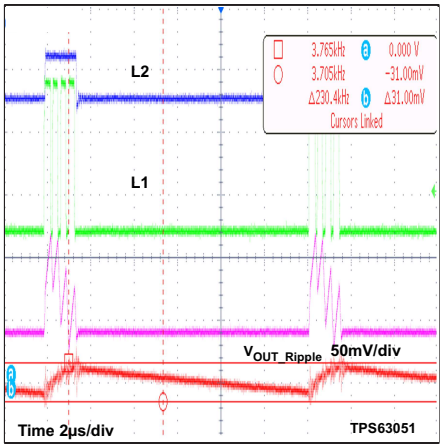
V_{IN} = 3.3 V I_{OUT} = 145 mA

Figure 23. Output Voltage ripple in Buck-Boost mode and PFM to PWM transition



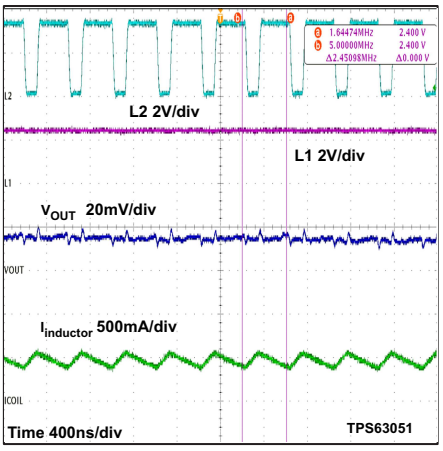
V_{IN} = 2.8 V I_{OUT} = 16 mA

Figure 24. Output Voltage Ripple in Boost Mode and PFM to PWM Transition



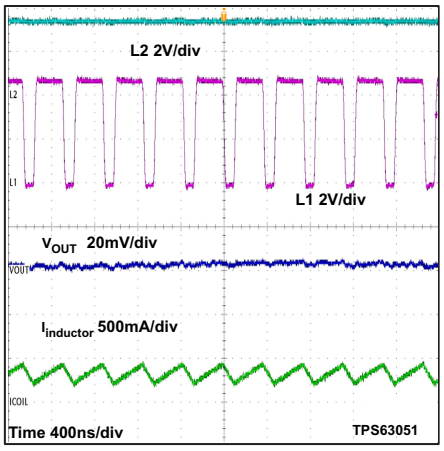
V_{IN} = 4.2 V I_{OUT} = 16 mA

Figure 25. Output Voltage Ripple in Buck Mode and PFM to PWM Transition



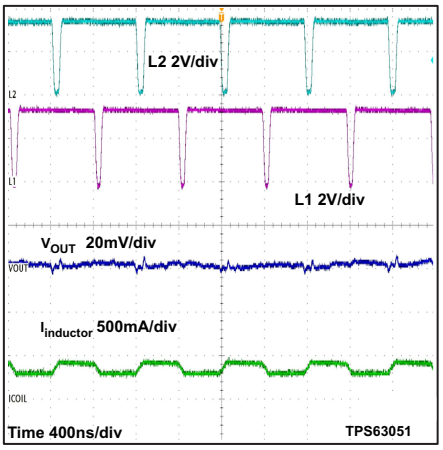
V_{IN} = 2.5 V I_{OUT} = 300 mA

Figure 26. Switching Waveform in Boost Mode and PWM



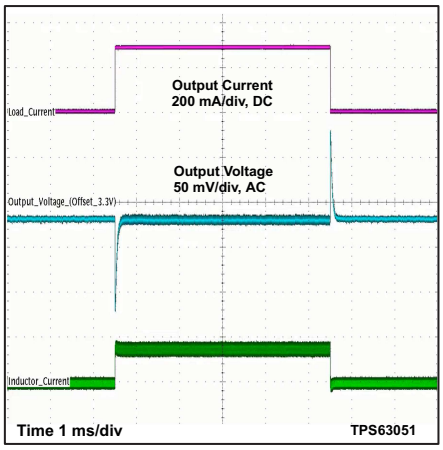
V_{IN} = 4.5 V I_{OUT} = 300 mA

Figure 27. Switching Waveform in Buck Mode and PWM



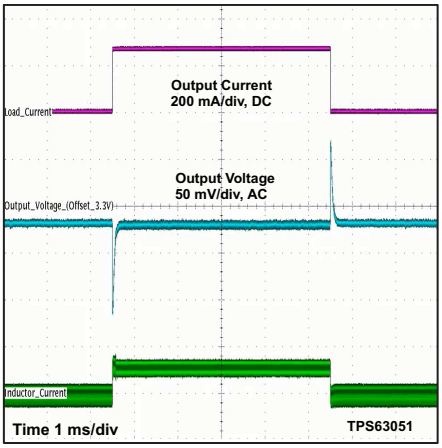
V_{IN} = 3.4 V I_{OUT} = 300 mA

Figure 28. Switching Waveform in Buck-Boost Mode and PWM



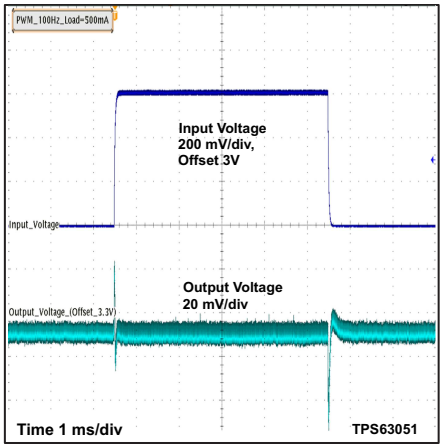
V_{IN} = 2.8 V Load change from 0 mA to 300 mA

Figure 29. Load Transient Response



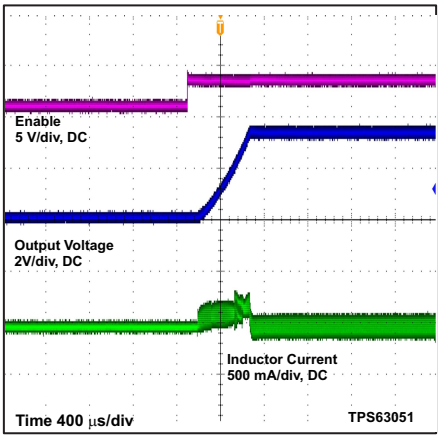
V_{IN} = 3.6 V Load change from 0 mA to 300 mA

Figure 30. Load Transient Response



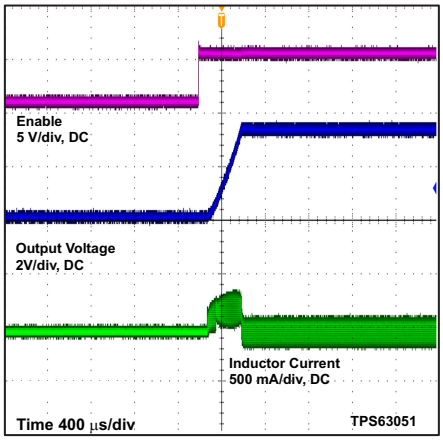
V_{OUT} = 3.3 V I_{OUT} = 500 mA

Figure 31. Line Transient Response



V_{OUT} = 3.3 V V_{IN} = 2.5 V I_{OUT} = 0 mA

Figure 32. Start Up After Enable



V_{OUT} = 3.3 V V_{IN} = 4.2 V I_{OUT} = 0 mA

Figure 33. Start Up After Enable

10 Power Supply Recommendations

The TPS6305x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6305x devices.

11 Layout

11.1 Layout Guidelines

The PCB layout is an important step to maintain the high performance of the TPS6305x devices.

- Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Routing wide and direct traces to the input and output capacitor results in low-trace resistance and low parasitic inductance.
- Use a common-power GND.
- The sense trace connected to FB is signal trace. Keep these traces away from L1 and L2 nodes.
- For the HotRod package option it is important to add a capacitor between FB node and ground to filter ground noise and to match efficiency results documented in these datasheet.

11.2 Layout Example (WCSP)

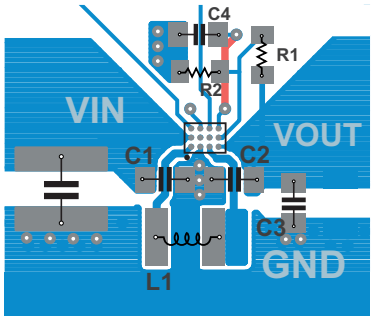


Figure 34. TPS6305x Layout (WCSP)

11.3 Layout Example (HotRod)

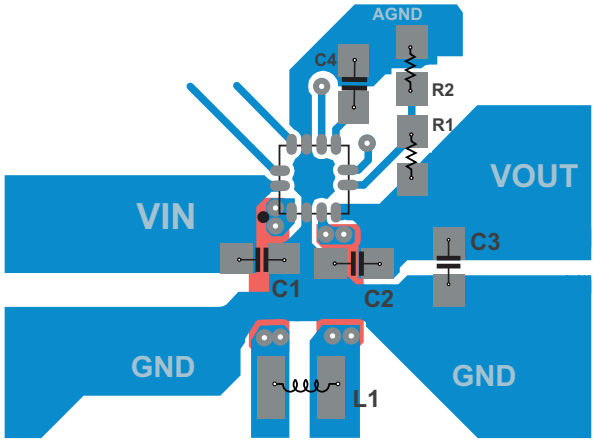


Figure 35. TPS6305x Layout (HotRod)

11.4 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the powerdissipation limits of a given component.

Two basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application notes: *Thermal Characteristics* (SZZA017), and *Semiconductor and IC Package Thermal Metrics* (SPRA953)

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 6. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS63050	Click here	Click here	Click here	Click here	Click here
TPS63051	Click here	Click here	Click here	Click here	Click here

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS63050RMWR	ACTIVE	VQFN-HR	RMW	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	F630	Samples
TPS63050RMWT	ACTIVE	VQFN-HR	RMW	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	F630	Samples
TPS63050YFFR	ACTIVE	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63050	Samples
TPS63050YFFT	ACTIVE	DSBGA	YFF	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63050	Samples
TPS63051RMWR	ACTIVE	VQFN-HR	RMW	12	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	F631	Samples
TPS63051RMWT	ACTIVE	VQFN-HR	RMW	12	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	F631	Samples
TPS63051YFFR	ACTIVE	DSBGA	YFF	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63051	Samples
TPS63051YFFT	ACTIVE	DSBGA	YFF	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	63051	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

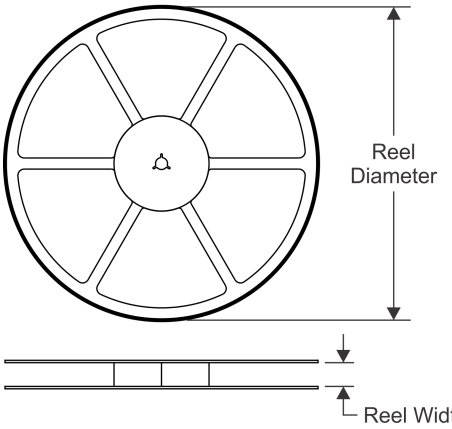
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

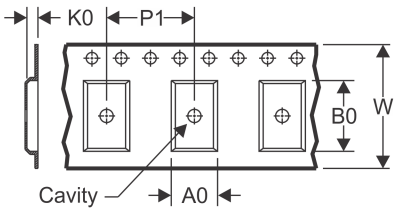
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

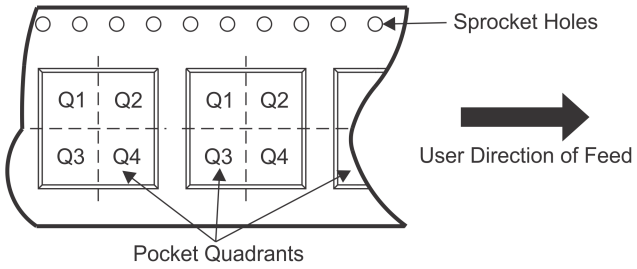


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

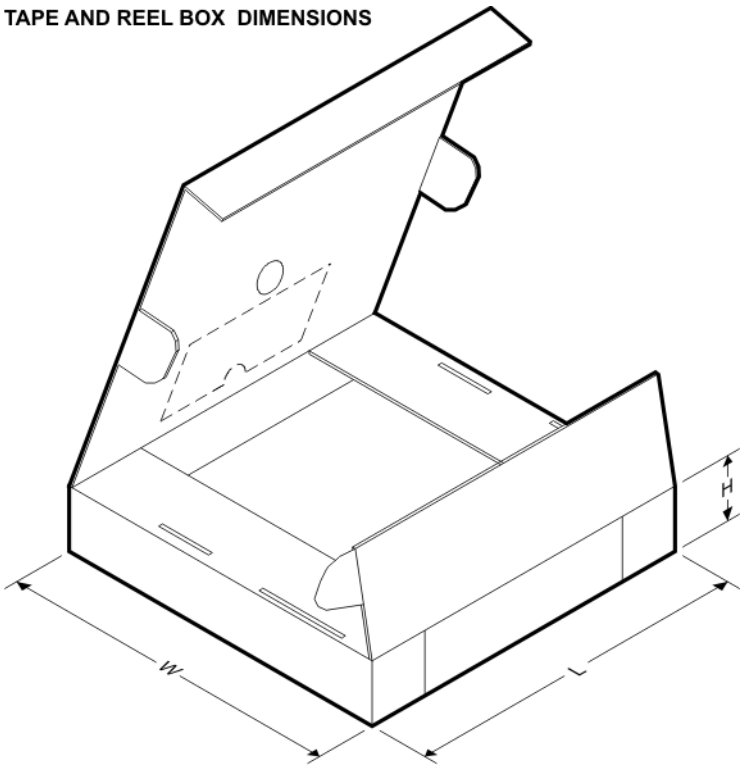
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

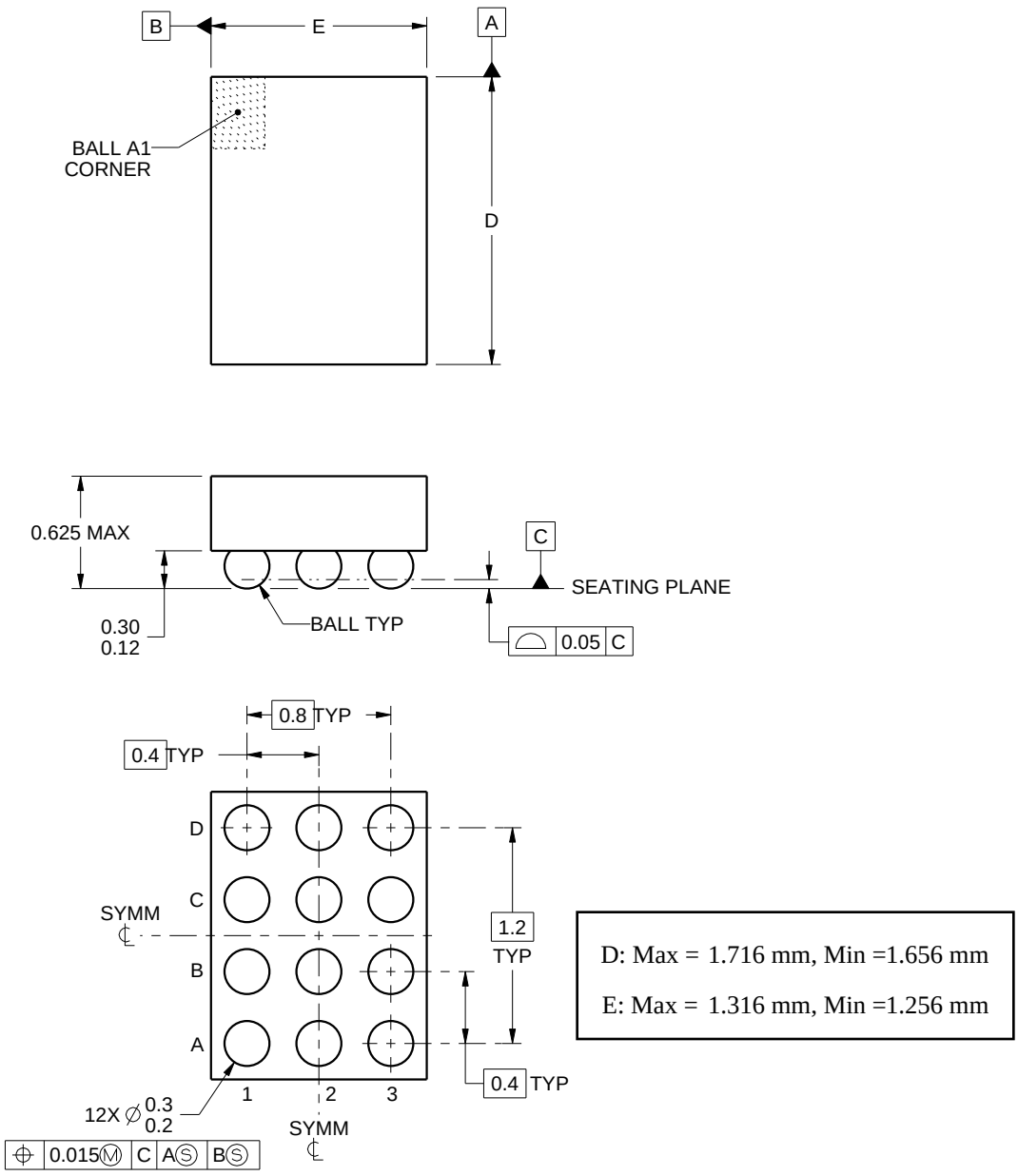
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS63050RMWR	VQFN-HR	RMW	12	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63050RMWT	VQFN-HR	RMW	12	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63050YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63050YFFT	DSBGA	YFF	12	250	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63051RMWR	VQFN-HR	RMW	12	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63051RMWT	VQFN-HR	RMW	12	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS63051YFFR	DSBGA	YFF	12	3000	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1
TPS63051YFFT	DSBGA	YFF	12	250	180.0	8.4	1.39	1.79	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

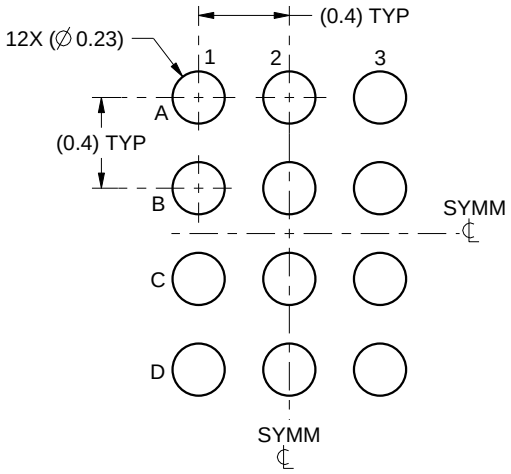
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS63050RMWR	VQFN-HR	RMW	12	3000	182.0	182.0	20.0
TPS63050RMWT	VQFN-HR	RMW	12	250	182.0	182.0	20.0
TPS63050YFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TPS63050YFFT	DSBGA	YFF	12	250	182.0	182.0	20.0
TPS63051RMWR	VQFN-HR	RMW	12	3000	182.0	182.0	20.0
TPS63051RMWT	VQFN-HR	RMW	12	250	182.0	182.0	20.0
TPS63051YFFR	DSBGA	YFF	12	3000	182.0	182.0	20.0
TPS63051YFFT	DSBGA	YFF	12	250	182.0	182.0	20.0



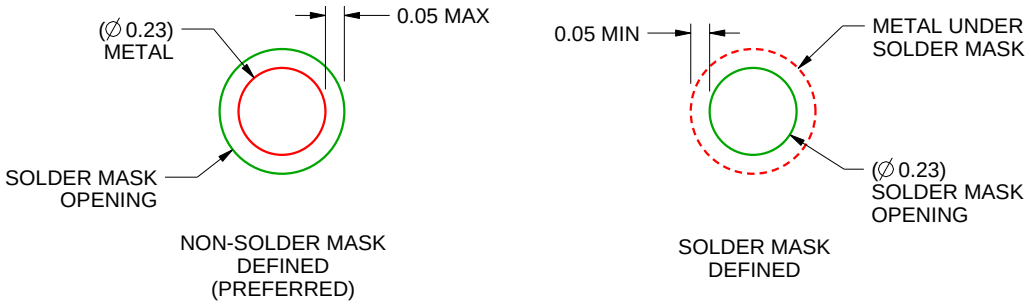
4222191/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

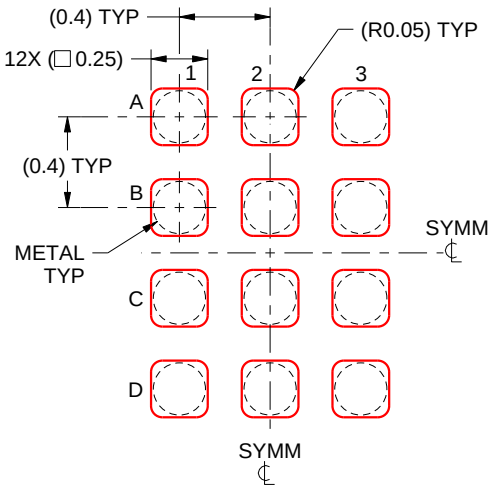


SOLDER MASK DETAILS
NOT TO SCALE

4222191/A 07/2015

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

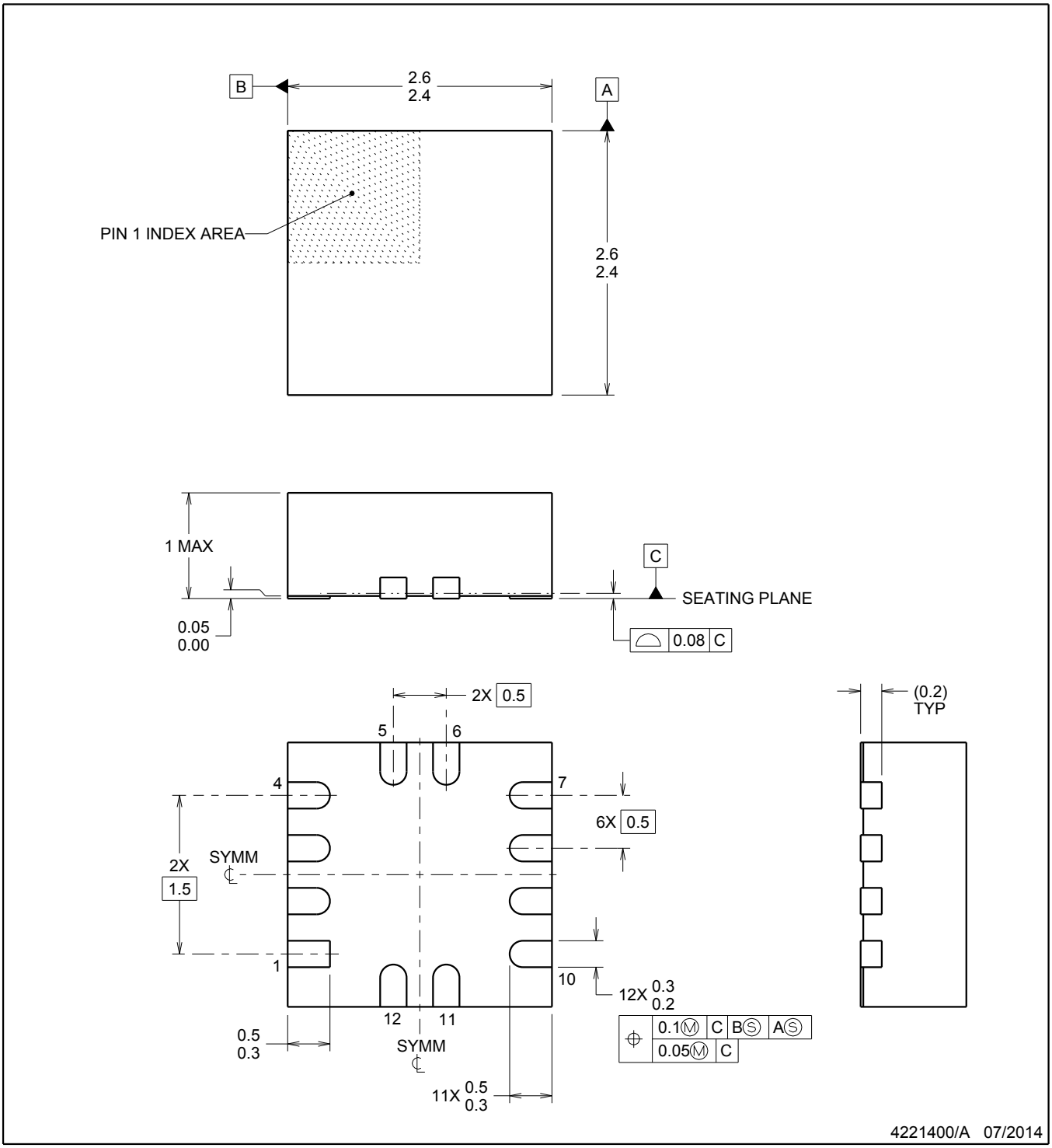


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222191/A 07/2015

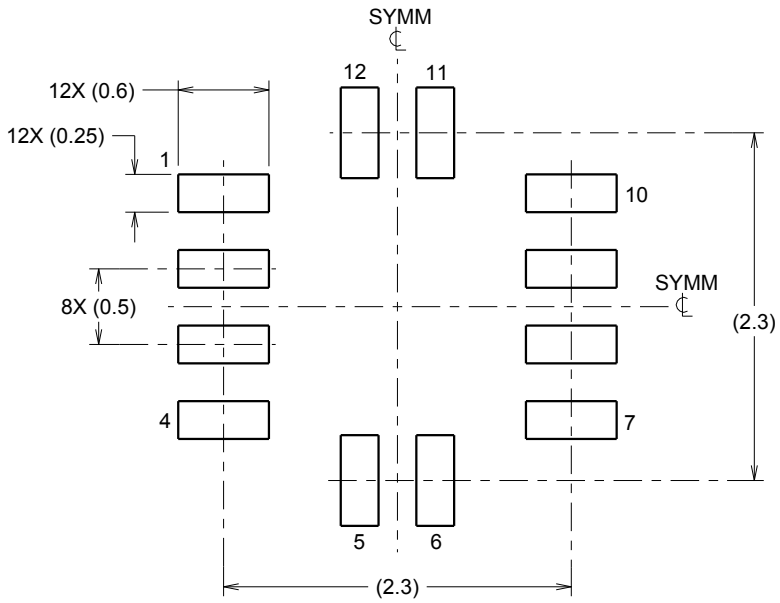
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

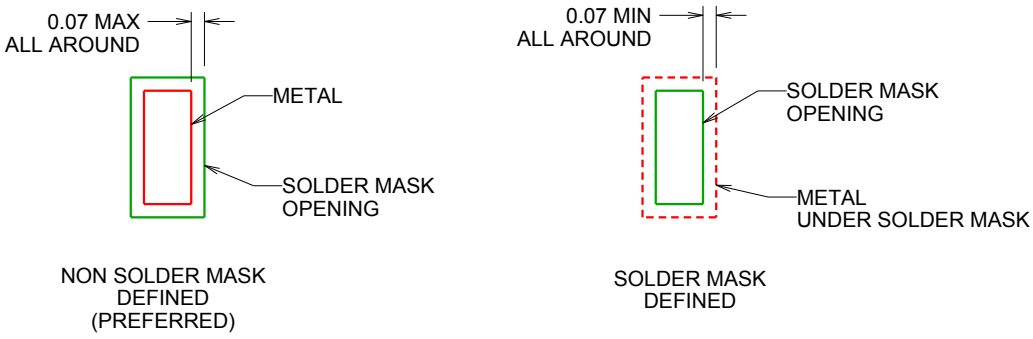


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:20X

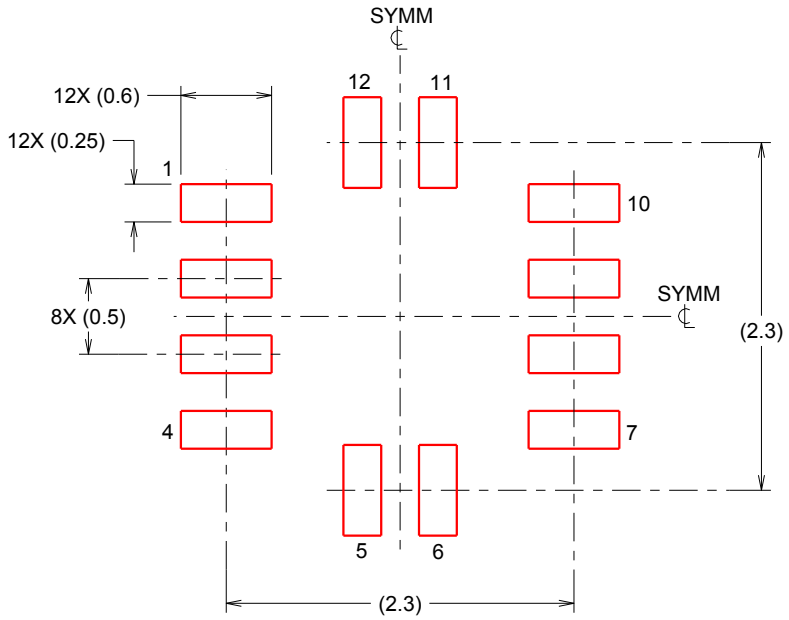


SOLDER MASK DETAILS

4221400/A 07/2014

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:20X

4221400/A 07/2014

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265