

74AVC16245

16-bit transceiver with direction pin; 3.6 V tolerant; 3-state

Rev. 3 — 31 January 2013

Product data sheet

1. General description

The 74AVC16245 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features two output enable inputs ($\overline{\text{nOE}}$) for easy cascading and two send/receive inputs ($\overline{\text{nDIR}}$) for direction control. Inputs $\overline{\text{nOE}}$ control the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74AVC16245 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, tie pins $\overline{\text{nOE}}$ to V_{CC} through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see [Figure 4](#) and [Figure 5](#))

2. Features and benefits

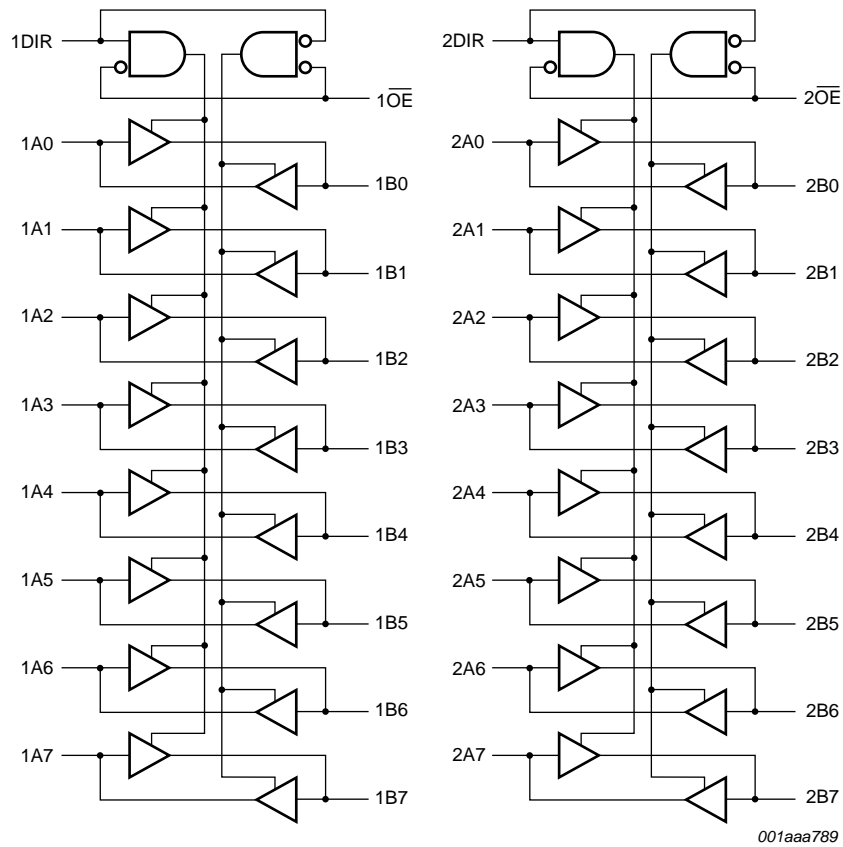
- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
 - ◆ JESD8-7 (1.2 V to 1.95 V)
 - ◆ JESD8-5 (1.8 V to 2.7 V)
 - ◆ JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple VCC and GND pins to minimize noise and ground bounce
- Supports Live Insertion

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|---------------|-------------------|---------|---|----------|
| | Temperature range | Name | Description | |
| 74AVC16245DGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

4. Functional diagram



001aaa789

Fig 1. Logic symbol

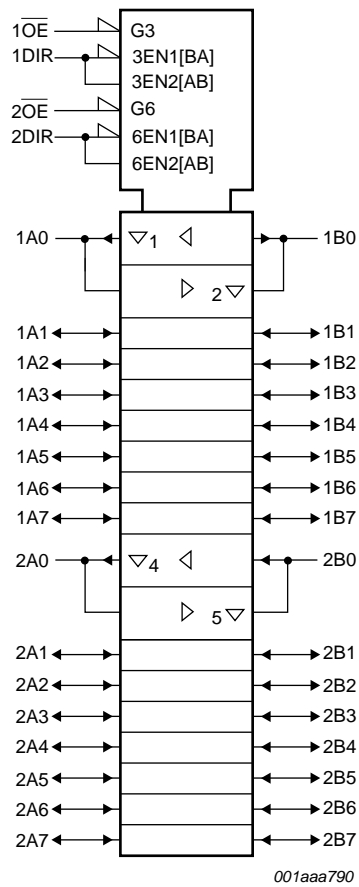
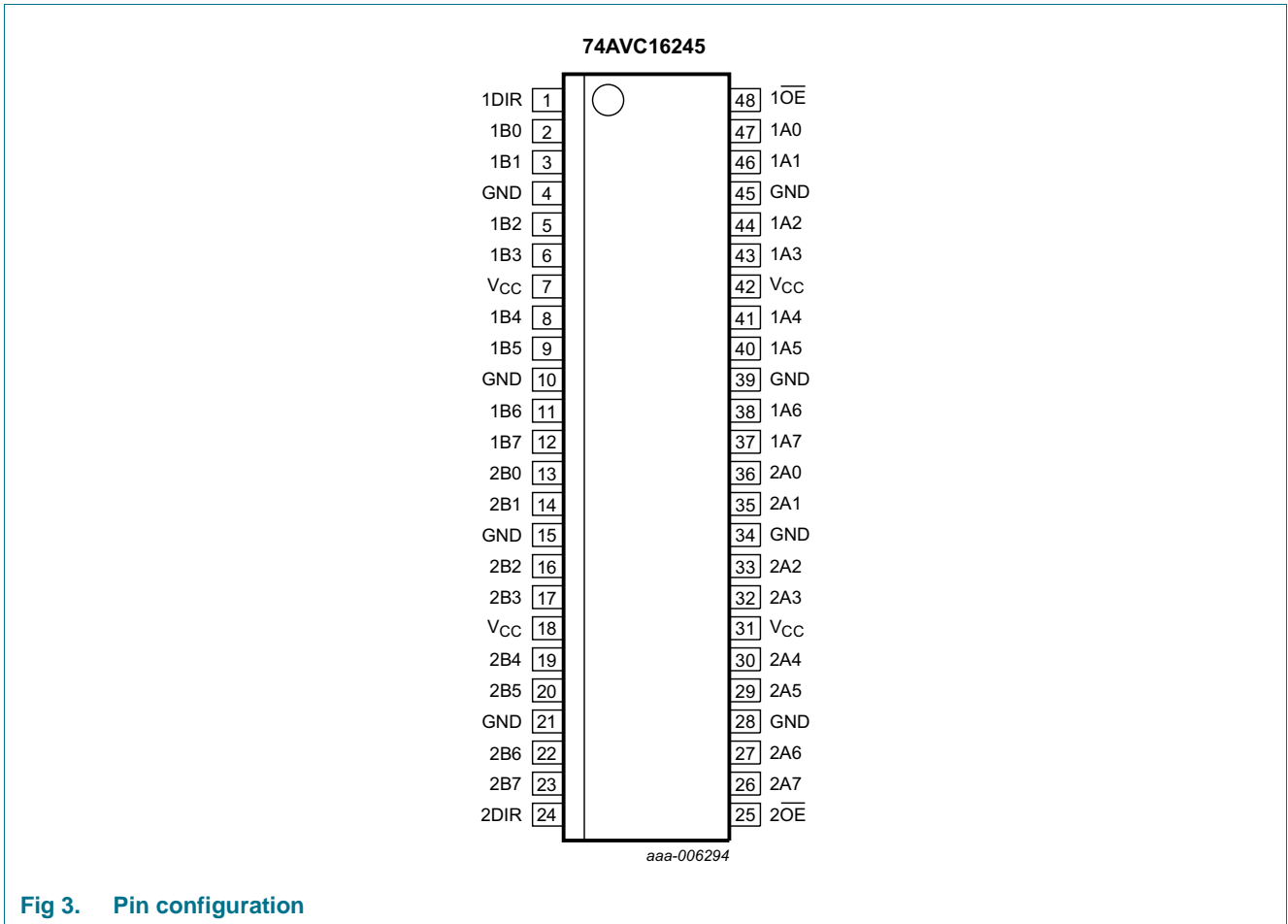


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|---|--------------------------------|----------------------------------|
| 1DIR, 2DIR | 1, 24 | direction control input |
| 1B0 to 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | data input/output |
| 2B0 to 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| V _{CC} | 7, 18, 31, 42 | supply voltage |
| 1 $\overline{\text{OE}}$, 2 $\overline{\text{OE}}$ | 48, 25 | output enable input (active LOW) |
| 1A0 to 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input/output |
| 2A0 to 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input/output |

6. Functional description

Table 3. Function table^[1]

| Inputs | | Outputs | |
|--------|------|---------|--------|
| nOE | nDIR | nAn | nBn |
| L | L | A = B | inputs |
| L | H | inputs | B = A |
| H | X | Z | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|----------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| I _{IK} | input clamping current | V _I < 0 V | -50 | - | mA |
| V _I | input voltage | | [1] -0.5 | +4.6 | V |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| V _O | output voltage | output HIGH or LOW | [1] -0.5 | V _{CC} + 0.5 | V |
| | | output 3-state | [1] -0.5 | +4.6 | V |
| I _O | output current | V _O = 0 V to V _{CC} | - | ±50 | mA |
| I _{CC} | supply current | | - | 100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C | [2] - | 500 | mW |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C, the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|--|------|-----|-----------------|------|
| V _{CC} | supply voltage | according to JEDEC Low Voltage Standards | 1.4 | - | 1.6 | V |
| | | | 1.65 | - | 1.95 | V |
| | | | 2.3 | - | 2.7 | V |
| | | | 3.0 | - | 3.6 | V |
| | | for low-voltage applications | 1.2 | - | 3.6 | V |
| V _I | input voltage | | 0 | - | 3.6 | V |
| V _O | output voltage | output HIGH or LOW | 0 | - | V _{CC} | V |
| | | output 3-state | 0 | - | 3.6 | V |
| T _{amb} | ambient temperature | in free air | -40 | - | +85 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 1.4 V to 1.6 V | 0 | - | 40 | ns/V |
| | | V _{CC} = 1.65 V to 1.95 V | 0 | - | 30 | ns/V |
| | | V _{CC} = 2.3 V to 3.0 V | 0 | - | 20 | ns/V |
| | | V _{CC} = 3.0 V to 3.6 V | 0 | - | 10 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|---|---------------------------|---|------------------------|------------------------|------------------------|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.2 V | V _{CC} | - | - | V |
| | | V _{CC} = 1.4 V to 1.6 V | 0.65 × V _{CC} | 0.9 | - | V |
| | | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | 0.9 | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | 1.2 | - | V |
| | | V _{CC} = 3.0 V to 3.6 V | 2.0 | 1.5 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.2 V | - | - | GND | V |
| | | V _{CC} = 1.4 V to 1.6 V | - | 0.9 | 0.35 × V _{CC} | V |
| | | V _{CC} = 1.65 V to 1.95 V | - | 0.9 | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | 1.2 | 0.7 | V |
| | | V _{CC} = 3.0 V to 3.6 V | - | 1.5 | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V | V _{CC} - 0.20 | V _{CC} | - | V |
| | | I _O = -3 mA; V _{CC} = 1.4 V | V _{CC} - 0.35 | V _{CC} - 0.21 | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | V _{CC} - 0.45 | V _{CC} - 0.25 | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | V _{CC} - 0.55 | V _{CC} - 0.37 | - | V |
| | | I _O = -12 mA; V _{CC} = 3.0 V | V _{CC} - 0.70 | V _{CC} - 0.47 | - | V |

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|------------------|---------------------------|---|-----|--------------------|------|------|
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V | - | GND | 0.20 | V |
| | | I _O = 3 mA; V _{CC} = 1.4 V | - | 0.22 | 0.35 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | 0.24 | 0.45 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | 0.38 | 0.55 | V |
| | | I _O = 12 mA; V _{CC} = 3.0 V | - | 0.53 | 0.70 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 1.4 V to 3.6 V | - | 0.1 | 2.5 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 3.6 V; V _{CC} = 0.0 V | - | ±0.1 | ±10 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND | | | | |
| | | V _{CC} = 1.4 V to 2.7 V | - | 0.1 | 5 | μA |
| | | V _{CC} = 3.0 V to 3.6 V | - | 0.1 | 10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A | | | | |
| | | V _{CC} = 1.4 V to 2.7 V | - | 0.1 | 20 | μA |
| | | V _{CC} = 3.0 V to 3.6 V | - | 0.2 | 40 | μA |
| C _I | input capacitance | | - | 5.0 | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

9.1 Graphs

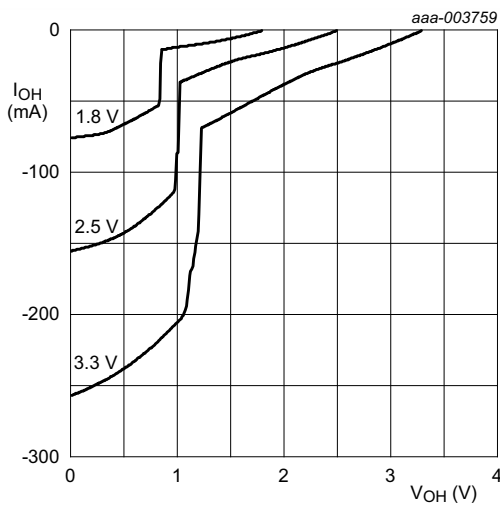


Fig 4. Output voltage as a function of the HIGH-level output current.

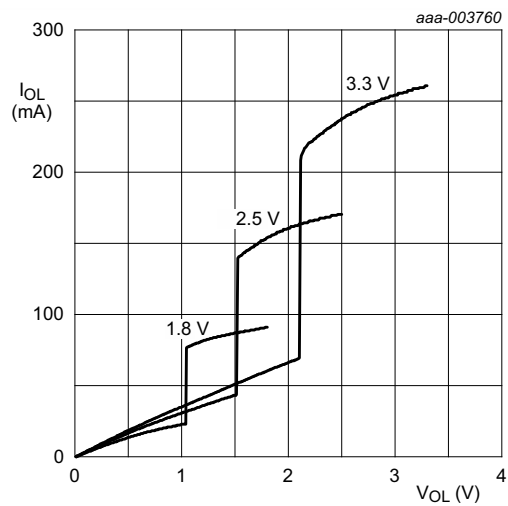


Fig 5. Output voltage as a function of the LOW-level output current.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | Unit |
|------------------|-------------------------------|---|------------------|--------------------|-----|------|
| | | | Min | Typ ^[2] | Max | |
| t _{pd} | propagation delay | nAn to nBn; nBn to nAn; see Figure 6 ^[1] | | | | |
| | | V _{CC} = 1.2 V | - | 2.8 | - | ns |
| | | V _{CC} = 1.4 V to 1.6 V | - | 1.8 | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 0.7 | 1.8 | 3.0 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.6 | 1.3 | 1.9 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.5 | 1.1 | 1.7 | ns |
| t _{en} | enable time | nOE to nAn, nBn; see Figure 7 ^[1] | | | | |
| | | V _{CC} = 1.2 V | - | 5.9 | - | ns |
| | | V _{CC} = 1.4 V to 1.6 V | - | 3.9 | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 1.4 | 3.3 | 6.5 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.4 | 4.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.7 | 2.0 | 3.7 | ns |
| t _{dis} | disable time | nOE to nAn, nBn; see Figure 7 ^[1] | | | | |
| | | V _{CC} = 1.2 V | - | 6.9 | - | ns |
| | | V _{CC} = 1.4 V to 1.6 V | - | 4.8 | - | ns |
| | | V _{CC} = 1.65 V to 1.95 V | 2.2 | 3.7 | 6.0 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.1 | 2.0 | 4.2 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.2 | 2.2 | 3.7 | ns |
| C _{PD} | power dissipation capacitance | per input; V _I = GND to V _{CC} ^[3] | | | | |
| | | outputs enabled | - | 42 | - | pF |
| | | outputs disabled | - | 2 | - | pF |

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

t_{en} is the same as t_{PZL} and t_{PZH}.

t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

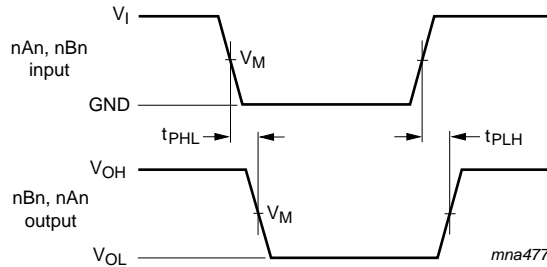
C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

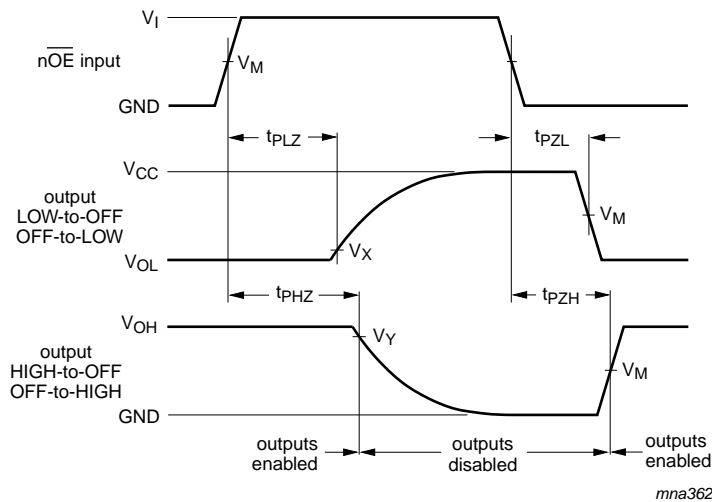
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11. Waveforms



Measurement points are given in [Table 8](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 6. The input (nAn, nBn) to output (nBn, nAn) propagation delays

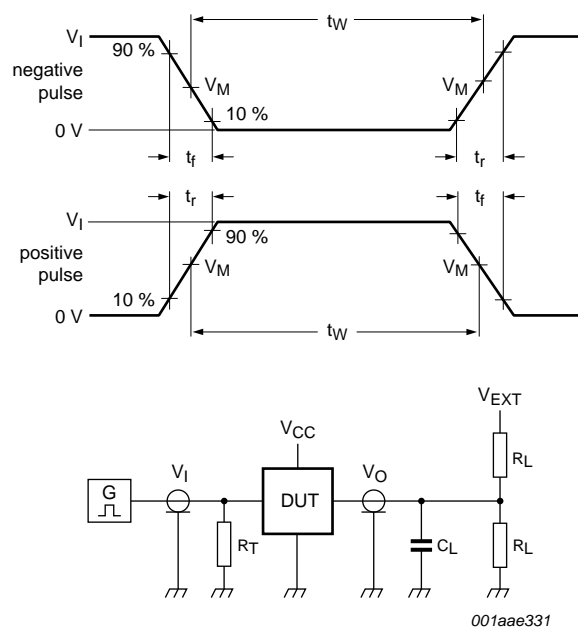


Measurement points are given in [Table 8](#).
 Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 7. 3-state enable and disable times

Table 8. Measurement points

| Supply voltage V_{CC} | V_M | Input | | | |
|----------------------------|---------------------|----------|-------------|-------------------|-------------------|
| | | V_I | $t_r = t_f$ | V_X | V_Y |
| 1.2 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 1.4 V to 1.6 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2 ns | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 3.0 V to 3.6 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2 ns | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 8. Test circuit for measuring switching times

Table 9. Test data

| Supply voltage | Input | | Load | | V_{EXT} | | |
|------------------|----------|-------------|-------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PLH}, t_{PHL} | t_{PLZ}, t_{PZL} | t_{PHZ}, t_{PZH} |
| 1.2 V | V_{CC} | ≤ 2 ns | 15 pF | 2 k Ω | open | $2 \times V_{CC}$ | GND |
| 1.4 V to 1.6 V | V_{CC} | ≤ 2 ns | 15 pF | 2 k Ω | open | $2 \times V_{CC}$ | GND |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2 ns | 30 pF | 1 k Ω | open | $2 \times V_{CC}$ | GND |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |
| 3.0 V to 3.6 V | V_{CC} | ≤ 2 ns | 30 pF | 500 Ω | open | $2 \times V_{CC}$ | GND |

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

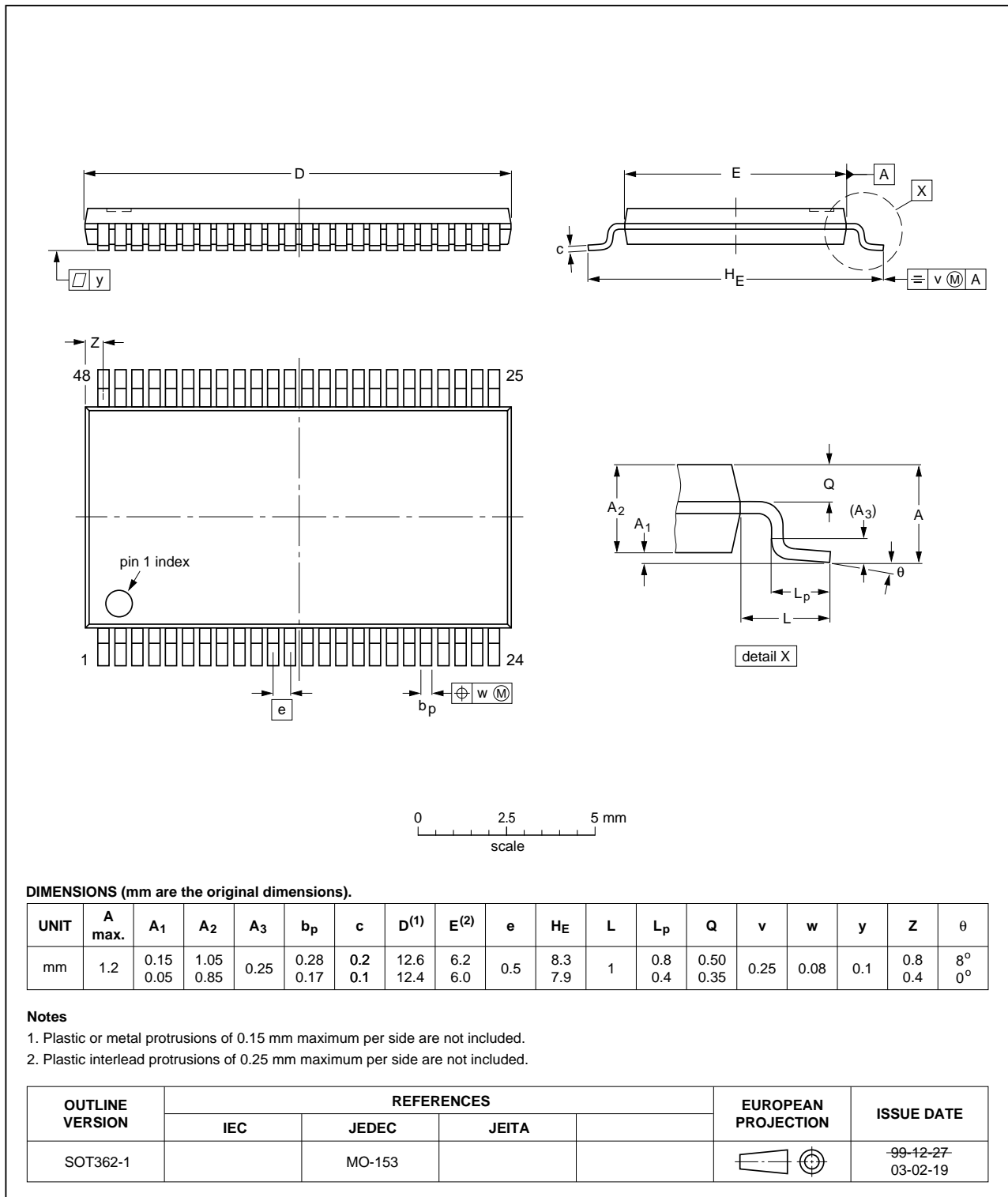


Fig 9. Package outline SOT362-1 (TSSOP48)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Order number | Supersedes |
|----------------|--------------|--|---------------|--------------|----------------|
| 74AVC16245 v.3 | 20130131 | Product data sheet | - | - | 74AVC16245 v.2 |
| Modifications: | | <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate. | | | |
| 74AVC16245 v.2 | 19991115 | Product specification | - | - | 74AVC16245 v.1 |
| 74AVC16245 v.1 | 19981211 | Product specification | - | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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