74LVT126

3.3 V quad buffer; 3-state

Rev. 5 — 14 June 2017 Product data sheet

1 General description

The LVT126 is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device combines low static and dynamic power dissipation with high speed and high output drive. The 74LVT126 device is a quad buffer that is ideal for driving bus lines. The device features four output enable inputs (1OE, 2OE, 3OE and 4OE), each controlling one of the 3-state outputs.

2 Features and benefits

- Quad bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- Latch-up protection:
  - JESD78: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - MM: exceeds 200 V

nexperia

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT126D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVT126DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74LVT126PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVT126BQ	-40 °C to +85 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4 Functional diagram

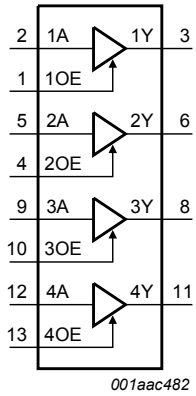


Figure 1. Logic symbol

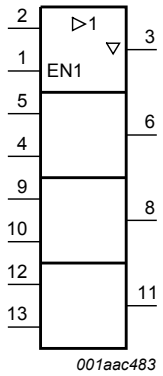


Figure 2. IEC logic symbol

5 Pinning information

5.1 Pinning

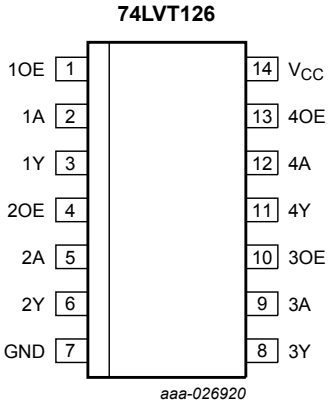


Figure 3. Pin configuration SO14

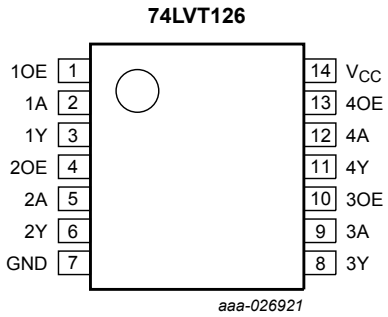
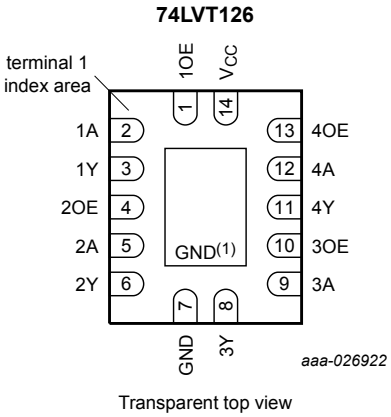


Figure 4. Pin configuration (T)SSOP14



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Figure 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE, 3OE, 4OE	1, 4, 10, 13	output enable inputs
1A, 2A, 3A, 4A	2, 5, 9, 12	data inputs
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data outputs
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6 Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nA	nY
H	L	L
H	H	H
L	X	Z

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	128	mA
		output in HIGH-state	-	-64	mA
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[2]	-	150	°C

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8 Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f ≥ 1 kHz	-	-	64	mA
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-1.2	-0.9	-	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_{CC} = 2.7 V to 3.6 V; I_{OH} = -100 µA	V_{CC} - 0.2	V_{CC} - 0.1	-	V
		V_{CC} = 2.7 V; I_{OH} = -8 mA	2.4	2.5	-	V
		V_{CC} = 3.0 V; I_{OH} = -32 mA	2.0	2.2	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V; I_{OL} = 100 µA	-	0.1	0.2	V
		V_{CC} = 2.7 V; I_{OL} = 24 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 16 mA	-	0.25	0.4	V
		V_{CC} = 3.0 V; I_{OL} = 32 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V; I_{OL} = 64 mA	-	0.4	0.55	V
I_I	input leakage current	all input pins				
		V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	1	10	µA
		control pins				
		V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	±0.1	±1	µA
		data pins				
		V_{CC} = 3.6 V; V_I = V_{CC} [2]	-	0.1	1	µA
		V_{CC} = 3.6 V; V_I = 0 V [2]	-	-1	-5	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	1	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3 V; V_I = 0.8 V	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3 V; V_I = 2.0 V	-75	-150	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 3.6 V; V_I = 0 V to 3.6 V [3]	-	-	-500	µA
I_{EX}	external current	output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.0 V	-	60	125	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; nOE = don't care [4]	-	±1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V				
		output HIGH: V_O = 3.0 V	-	1	5	µA
		output LOW: V_O = 0.5 V	-	-1	-5	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		outputs HIGH	-	0.13	0.19	mA
		outputs LOW	-	2	7	mA

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
		outputs disabled	[5]	-	0.13	0.19	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3 V to 3.6 V; one input at V_{CC} - 0.6 V and other inputs at V_{CC} or GND	[6]	-	0.1	0.2	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V		-	8	-	pF

[1] Typical values are measured at nominal V_{CC} and T_{amb} = 25 °C.
[2] Unused pins at V_{CC} or GND.
[3] This is the bus hold overdrive current required to force the input to the opposite logic state.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[5] Measured with outputs pulled up to V_{CC} or GND.
[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10 Dynamic characteristics

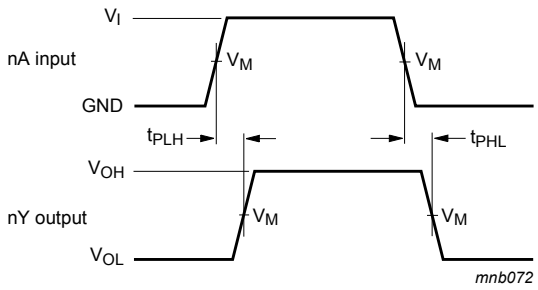
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
t_{PLH}	LOW to HIGH propagation delay	nA to nY; see Figure 6				
		V_{CC} = 2.7 V	-	-	4.5	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.3	3.8	ns
t_{PHL}	HIGH to LOW propagation delay	nA to nY; see Figure 6				
		V_{CC} = 2.7 V	-	-	4.4	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.4	3.9	ns
t_{PZH}	OFF-state to HIGH propagation delay	nOE to nY; see Figure 7				
		V_{CC} = 2.7 V	-	-	6.1	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	3.6	5.4	ns
t_{PZL}	OFF-state to LOW propagation delay	nOE to nY; see Figure 7				
		V_{CC} = 2.7 V	-	-	5.8	ns
		V_{CC} = 3.3 V ± 0.3 V	1.1	3.6	5.2	ns
t_{PHZ}	HIGH to OFF-state propagation delay	nOE to nY; see Figure 7				
		V_{CC} = 2.7 V	-	-	4.3	ns
		V_{CC} = 3.3 V ± 0.3 V	1.0	2.2	3.8	ns
t_{PLZ}	LOW to OFF-state propagation delay	nOE to nY; see Figure 7				
		V_{CC} = 2.7 V	-	-	6.1	ns
		V_{CC} = 3.3 V ± 0.3 V	1.3	3.6	5.5	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

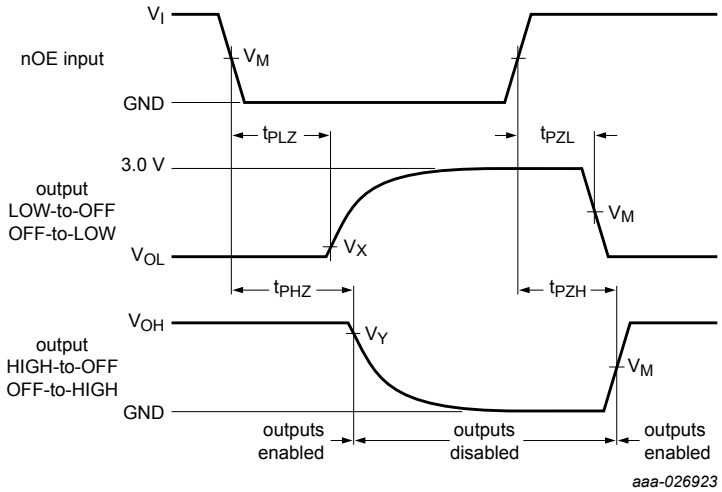
10.1 Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 6. Propagation delay input (nA) to output (nY)



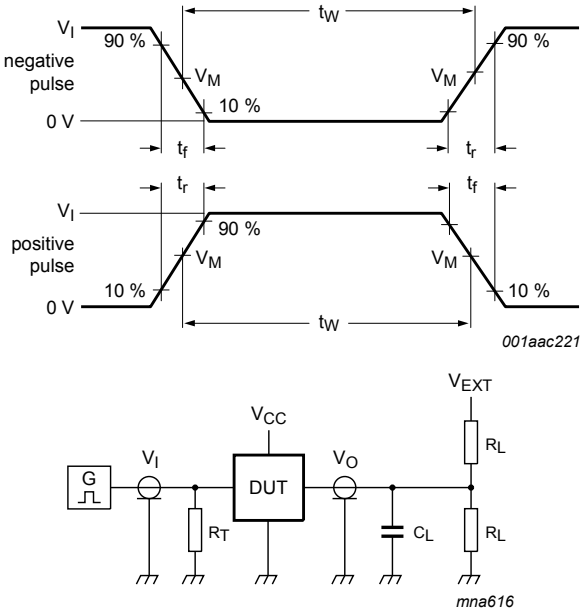
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 7. Enable and disable times of 3-state outputs

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

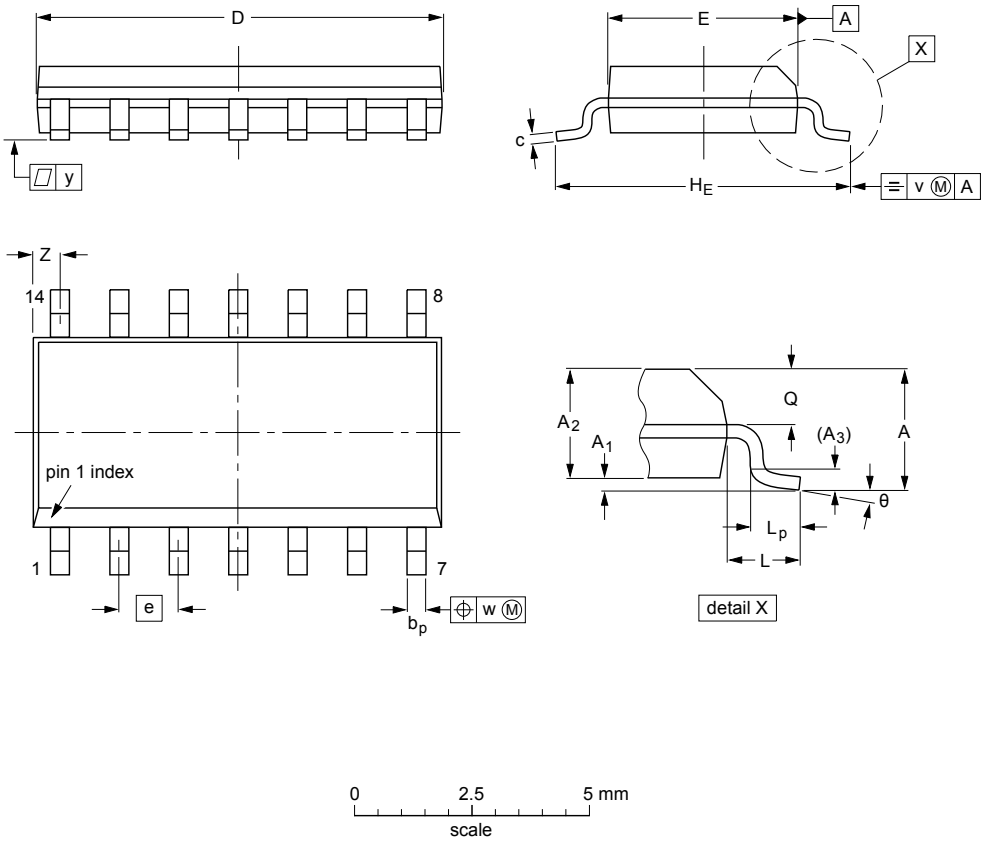
Figure 8. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11 Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

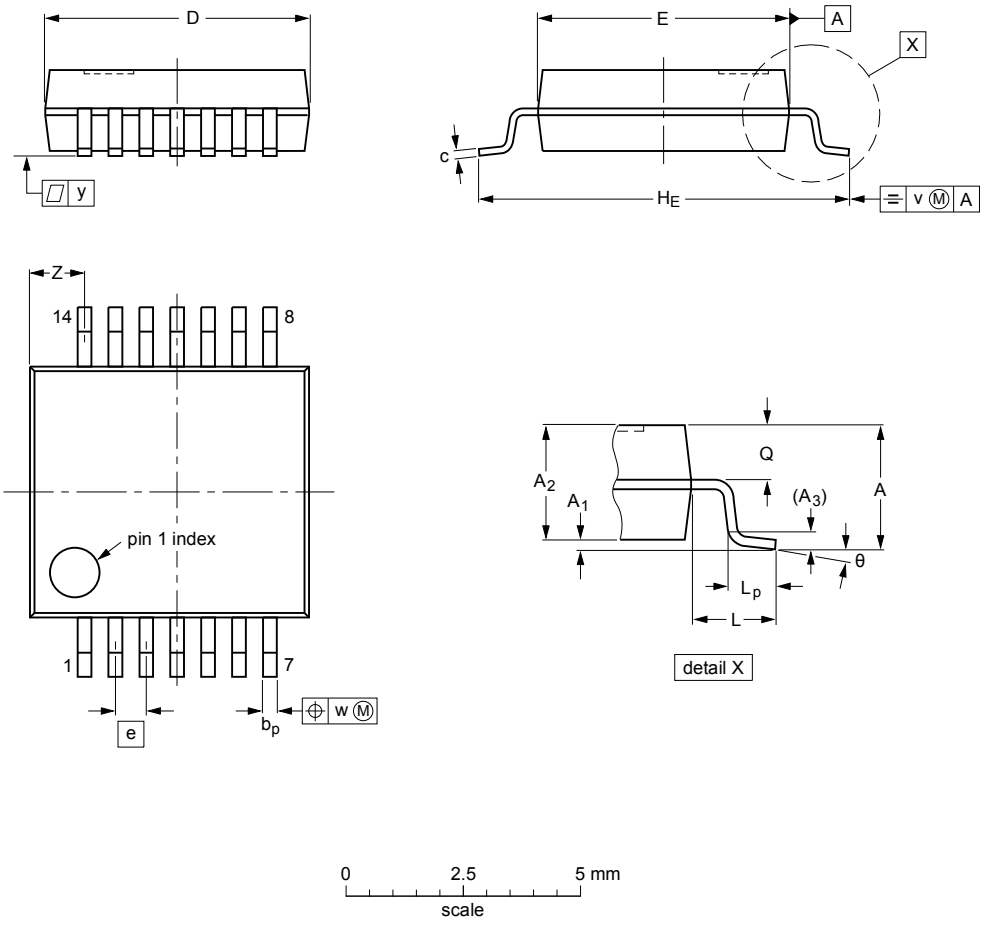
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Figure 9. Package outline SO14 (SOT108-1)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

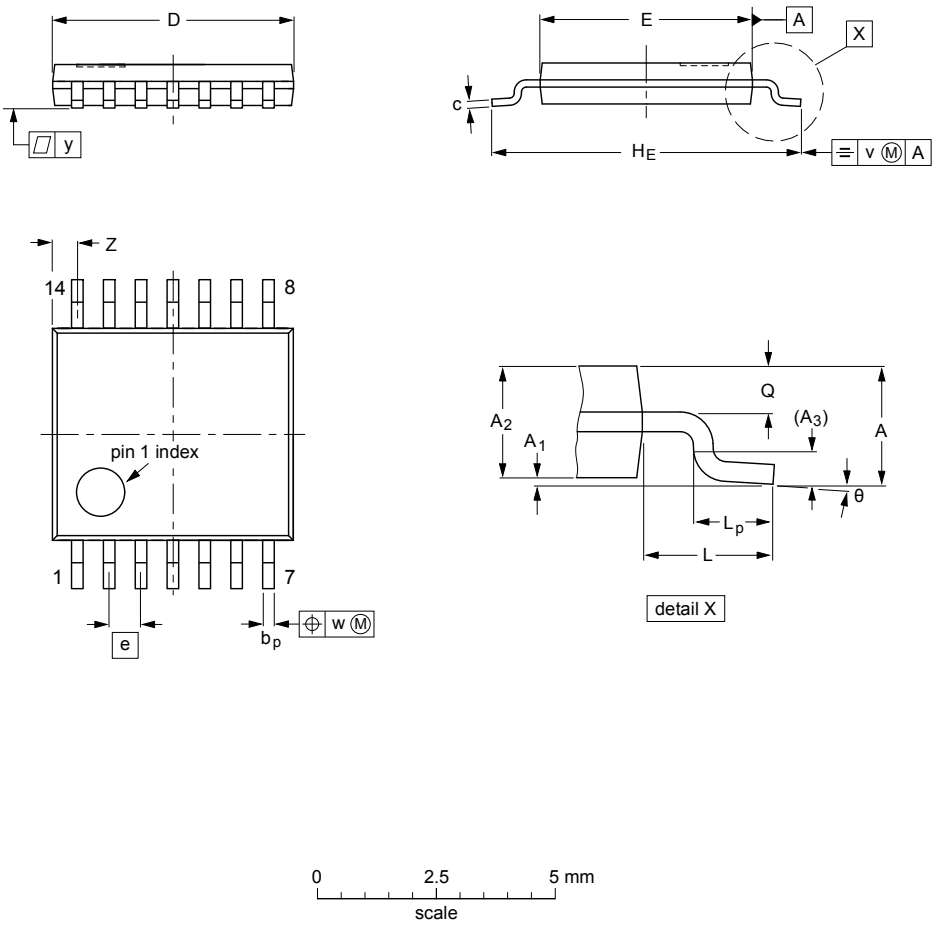
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Figure 10. Package outline SSOP14 (SOT337-1)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

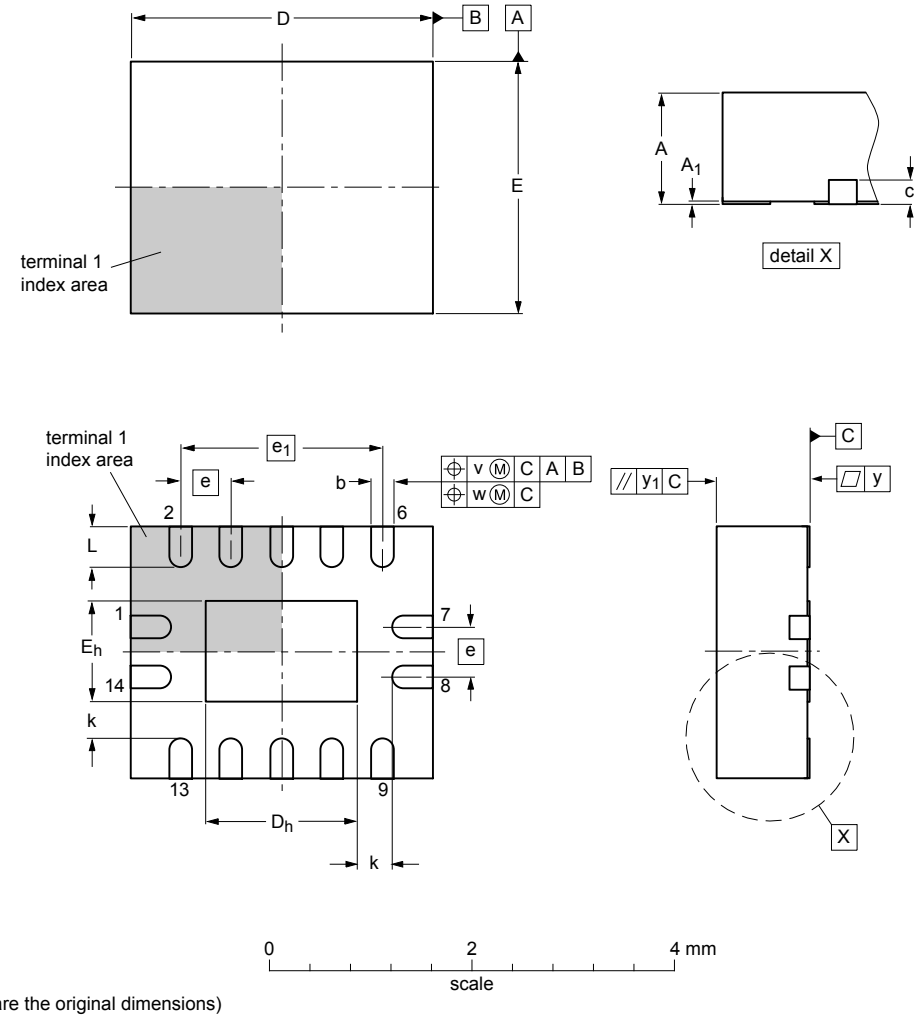
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Figure 11. Package outline TSSOP14 (SOT402-1)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm **SOT762-1**



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	k	L	v	w	y	y_1
	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
mm	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				~~15-04-10~~ 15-05-05

Figure 12. Package outline DHVQFN14 (SOT762-1)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT126_5	20170614	Product data sheet	-	74LVT126_4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVT126_4	20050211	Product data sheet	-	74LVT126_3
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Figure 5: added note 1.			
74LVT126_3	20040624	Product data sheet	-	74LVT126_2
74LVT126_2	19980219	Product specification	-	74LVT126_1
74LVT126_1	19951221	-	-	-

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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