74LVC1G10

Single 3-input NAND gate Rev. 5 — 28 November 2016

Product data sheet

1. **General description**

The 74LVC1G10 provides a low-power, low-voltage single 3-input NAND gate.

The inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device in a mixed 3.3 V and 5 V environment.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

Features and benefits 2.

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- Complies with JEDEC standard:
 - ◆ JESD8-7 (1.65 V to 1.95 V)
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8-B/JESD36 (2.7 V to 3.6 V).
- \pm 24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Inputs accept voltages up to 5 V
- ESD protection:
 - ♦ HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C



3. Ordering information

Table 1. Ordering information

Type number	Package	Package						
	Temperature range	Name	Description	Version				
74LVC1G10GW	-40 °C to +125 °C	SC-88	plastic surface-mounted package; 6 leads	SOT363				
74LVC1G10GV	-40 °C to +125 °C	SC-74	plastic surface-mounted package (TSOP6); 6 leads	SOT457				
74LVC1G10GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 \times 1.45 \times 0.5 mm	SOT886				
74LVC1G10GF	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm	SOT891				
74LVC1G10GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $0.9 \times 1.0 \times 0.35$ mm	SOT1115				
74LVC1G10GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body $1.0 \times 1.0 \times 0.35$ mm	SOT1202				

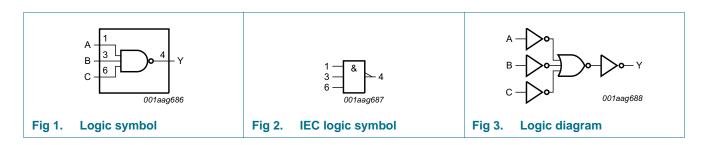
4. Marking

Table 2. Marking

Type number	Marking code ^[1]
74LVC1G10GW	YM
74LVC1G10GV	YM
74LVC1G10GM	YM
74LVC1G10GF	YM
74LVC1G10GN	YM
74LVC1G10GS	YM

^[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

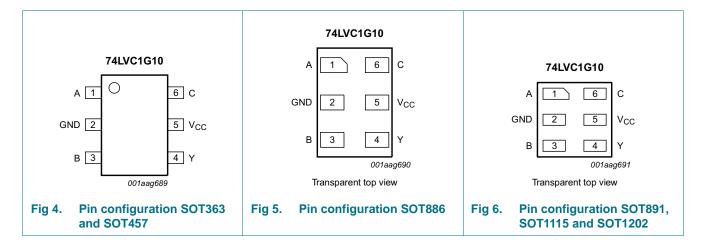
5. Functional diagram



Single 3-input NAND gate

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
A	1	data input
GND	2	ground (0 V)
В	3	data input
Υ	4	data output
V _{CC}	5	supply voltage
С	6	data input

7. Functional description

Table 4. Function table[1]

Input	Output		
A	В	С	Υ
Н	Н	Н	L
L	X	X	Н
X	L	X	Н
X	X	L	Н

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
VI	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 \text{ V}$	-	±50	mA
Vo	output voltage	Active mode [1][2]	-0.5	V _{CC} + 0.5	V
		Power-down mode [1][2]	-0.5	+6.5	V
Io	output current	$V_O = 0 \text{ V to } V_{CC}$	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	$T_{amb} = -40 ^{\circ}\text{C} \text{ to } +125 ^{\circ}\text{C}$	-	250	mW
T _{stg}	storage temperature		-65	+150	°C

^[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	Active mode	0	-	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	-	5.5	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

^[2] When $V_{CC} = 0 \text{ V}$ (Power-down mode), the output voltage can be 5.5 V in normal operation.

^[3] For SC-88 and SC-74A packages: above 87.5 °C the value of P_{tot} derates linearly with 4.0 mW/K. For XSON6 package: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °	°C to +8	5 °C	-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
	voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V_{IL}	LOW-level input	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
	voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = -100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	V _{CC} – 0.1	-	-	V _{CC} – 0.1	-	V
		$I_{O} = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	0.95	-	V
		$I_{O} = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.9	-	-	1.7	-	V
		$I_{O} = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	1.9	-	V
		$I_{O} = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.3	-	-	2.0	-	V
		$I_{O} = -32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.8	-	-	3.4	-	V
V_{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	$I_O = 100 \mu A;$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	-	0.10	-	0.10	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.70	V
		$I_{O} = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.30	-	0.45	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.40	-	0.60	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.80	V
		$I_O = 32 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.55	-	0.80	V
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	μА
I _{OFF}	power-off leakage current	V_{I} or $V_{O} = 5.5 \text{ V}; V_{CC} = 0 \text{ V}$	-	±0.1	±2	-	±2	μА
I _{CC}	supply current	$V_I = 5.5 \text{ V or GND}; I_O = 0 \text{ A};$ $V_{CC} = 1.65 \text{ V to } 5.5 \text{ V}$	-	0.1	4	-	4	μΑ
Δl _{CC}	additional supply current	$V_{I} = V_{CC} - 0.6 \text{ V}; I_{O} = 0 \text{ A}; V_{CC} = 2.3 \text{ V to 5.5 V}; per pin$	-	5	500	-	500	μΑ
Cı	input capacitance	$V_{CC} = 3.3 \text{ V};$ $V_{I} = \text{GND to } V_{CC}$	-	3	-	-	-	pF

^[1] All typical values are measured at T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Figure 8.

Symbol	Parameter	Conditions	-40	°C to +8	5 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	A, B and C to Y; see Figure 7						
		V _{CC} = 1.65 V to 1.95 V	1.5	4.7	18.0	1.5	21.5	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	3.0	6.5	1.0	7.8	ns
		V _{CC} = 2.7 V	1.0	3.0	6.0	1.0	7.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.6	5.0	1.0	6.2	ns
		V _{CC} = 4.5 V to 5.5 V	1.0	1.9	3.6	1.0	4.4	ns
C _{PD}	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}; V_{CC} = 3.3 \text{ V}$ [3]	-	12	-	-	-	pF

- [1] Typical values are measured at $T_{amb} = 25$ °C and $V_{CC} = 1.8$ V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
- [2] t_{pd} is the same as t_{PLH} and t_{PHL} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

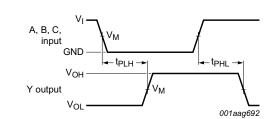
C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms



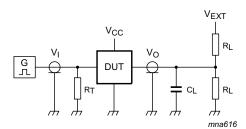
Measurement points are given in Table 9.

 $V_{\mbox{\scriptsize OL}}$ and $V_{\mbox{\scriptsize OH}}$ are typical output voltage levels that occur with the output load.

Fig 7. The input (A, B, C) to output (Y) propagation delays

Table 9. **Measurement points**

Supply voltage	Input	Output
Vcc	V _M	V _M
1.65 V to 1.95 V	0.5V _{CC}	0.5V _{CC}
2.3 V to 2.7 V	0.5V _{CC}	0.5V _{CC}
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	0.5V _{CC}	0.5V _{CC}



Test data is given in <u>Table 10</u>.

Definitions for test circuit:

 R_L = Load resistance.

 C_L = Load capacitance including jig and probe capacitance.

 R_T = Termination resistance should be equal to the output impedance Z_0 of the pulse generator.

 V_{EXT} = External voltage for measuring switching times.

Test circuit for measuring switching times Fig 8.

Table 10. Test data

Supply voltage	Input		Load		V _{EXT}
V _{CC}	VI	$t_r = t_f$	CL	R _L	t _{PLH} , t _{PHL}
1.65 V to 1.95 V	V _{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V _{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V _{CC}	≤ 2.5 ns	50 pF	500 Ω	open

13. Package outline

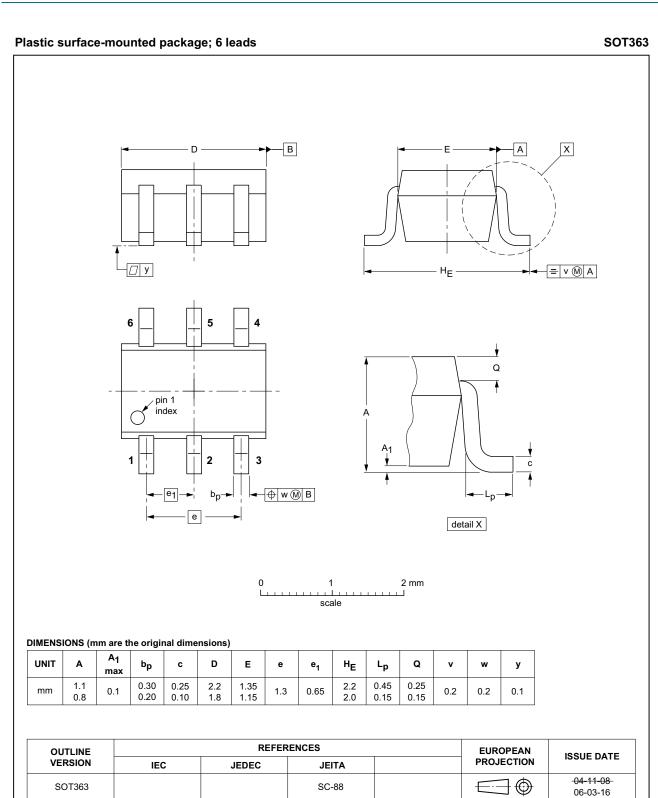


Fig 9. Package outline SOT363 (SC-88)

74LVC1G10

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Plastic surface-mounted package (TSOP6); 6 leads

SOT457

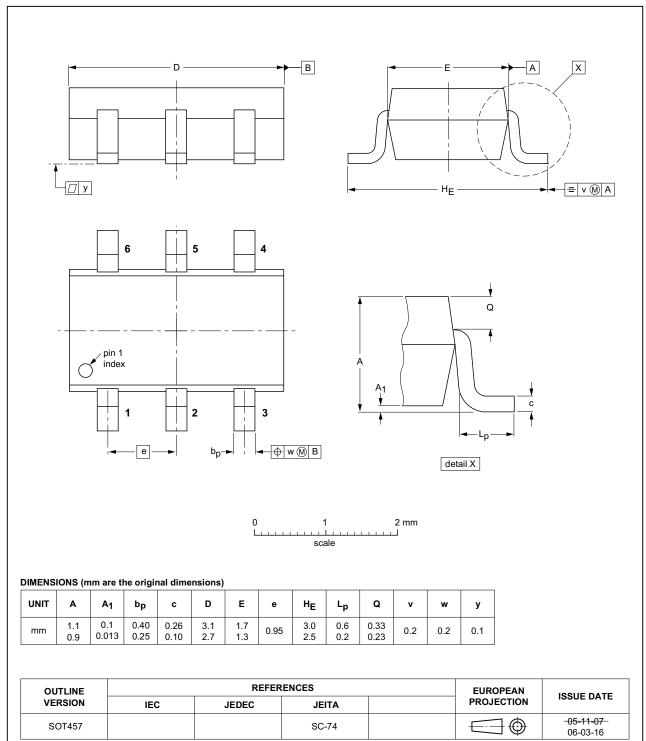


Fig 10. Package outline SOT457 (SC-74)

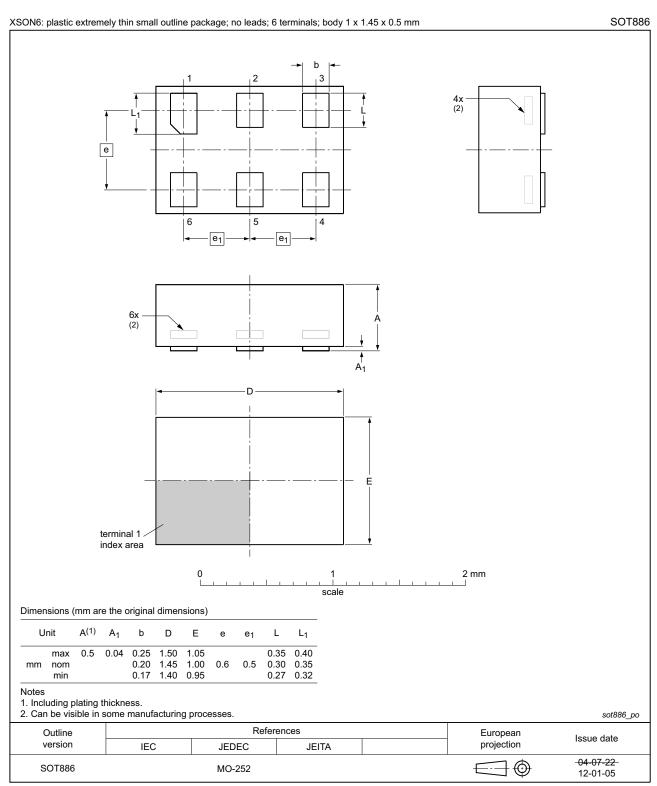


Fig 11. Package outline SOT886 (XSON6)

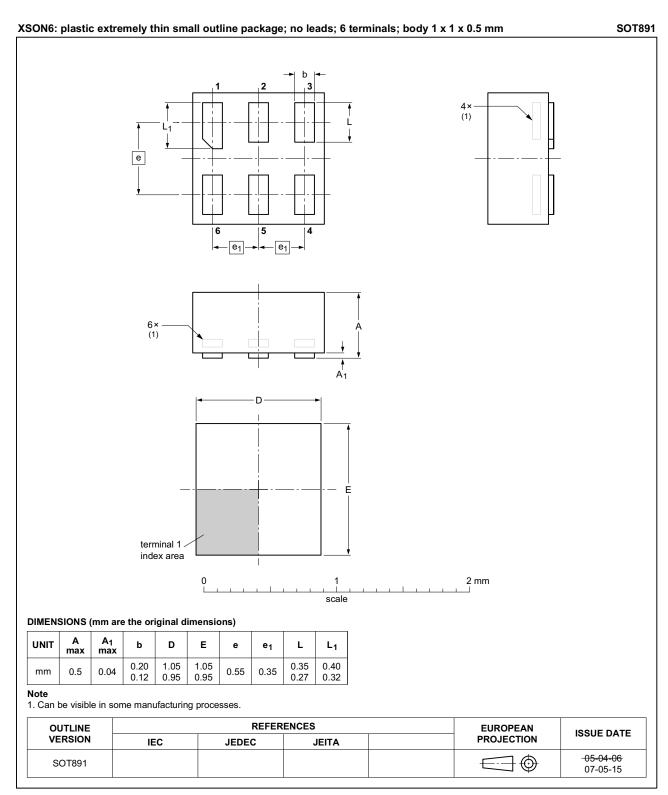


Fig 12. Package outline SOT891 (XSON6)

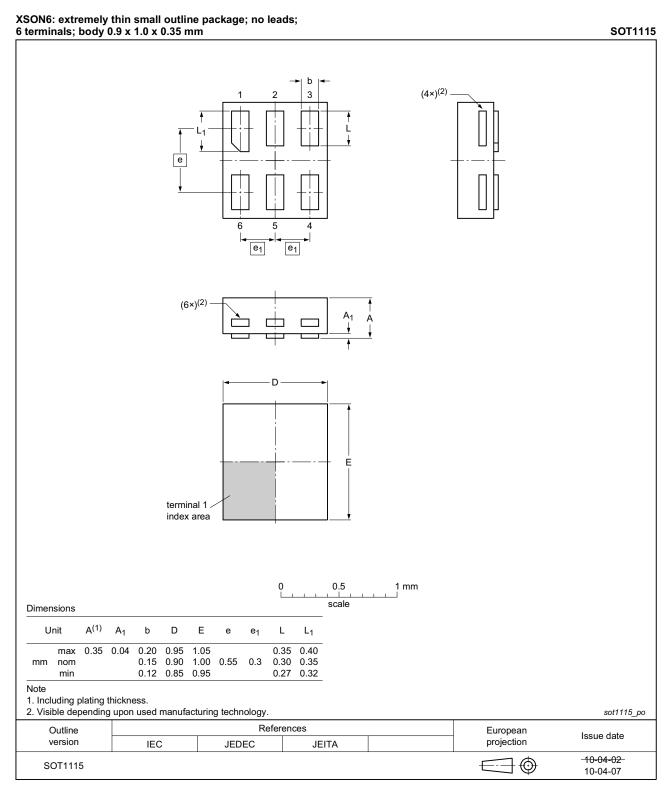


Fig 13. Package outline SOT1115 (XSON6)

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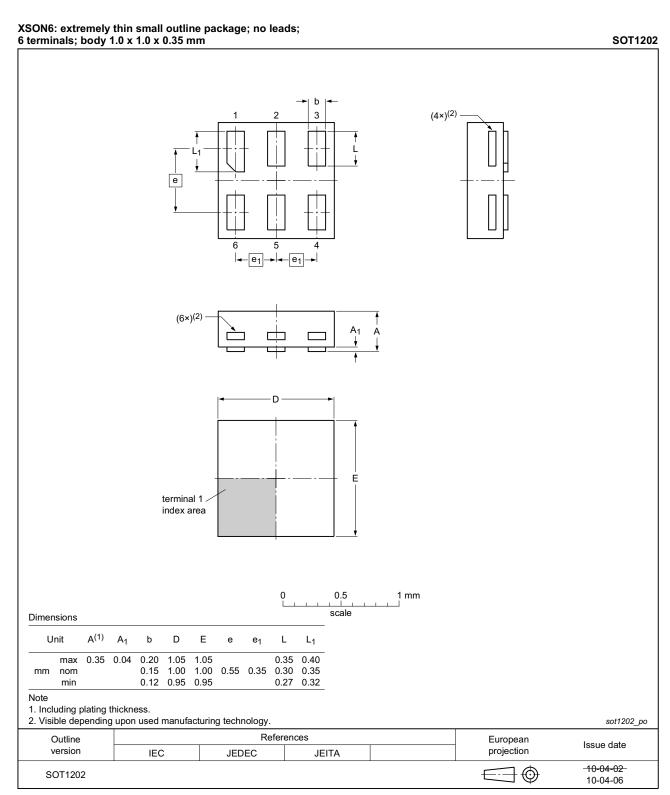


Fig 14. Package outline SOT1202 (XSON6)

Single 3-input NAND gate

14. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes		
74LVC1G10 v.5	20161128	Product data sheet	-	74LVC1G10 v.4		
Modifications:	• <u>Table 7</u> : The	• Table 7: The maximum limits for leakage current and supply current have changed.				
74LVC1G10 v.4	20140910	Product data sheet	-	74LVC1G10 v.3		
Modifications:	Package out	line drawing of SOT886 (Figur	e 11) modified.	1		
74LVC1G10 v.3	20111208	Product data sheet	-	74LVC1G10 v.2		
74LVC1G10 v.2	20101021	Product data sheet	-	74LVC1G10 v.1		
74LVC1G10 v.1	20071002	Product data sheet	-	-		

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Single 3-input NAND gate

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