

CD74HC4051-Q1 ANALOG MULTIPLEXER/DEMULTIPLEXER

SCLS552A – DECEMBER 2003 – REVISED APRIL 2008

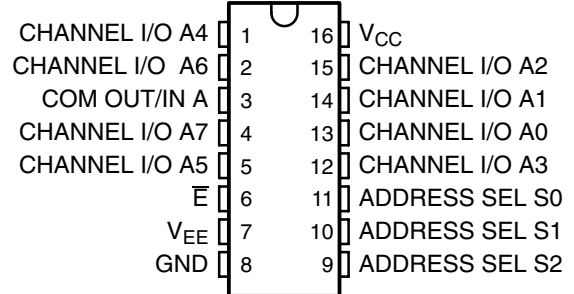
- **Qualified for Automotive Applications**
- **Wide Analog Input Voltage Range of ± 5 V Max**
- **Low ON Resistance**
 - 70 Ω Typical ($V_{CC} - V_{EE} = 4.5$ V)
 - 40 Ω Typical ($V_{CC} - V_{EE} = 9$ V)
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **Break-Before-Make Switching**
- **Operation Control Voltage = 2 V to 6 V**
- **Switch Voltage = 0 V to 10 V**
- **High Noise Immunity $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} , $V_{CC} = 5$ V**

description/ordering information

This device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). These bidirectional switches allow any analog input to be used as an output and vice versa. The switches have low ON resistance and low OFF leakages. In addition, the device has an enable control (\bar{E}) that, when high, disables all switches to their OFF state.

M OR PW PACKAGE
(TOP VIEW)



ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
	SOIC – M	Tape and reel		
–40°C to 125°C	SOIC – M	Tape and reel	CD74HC4051QM96Q1	HC4051Q
	TSSOP – PW	Tape and reel	CD74HC4051QPWRQ1	HJ4051Q

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at <http://www.ti.com>.

‡ Package drawings, thermal data, and symbolization are available at <http://www.ti.com/packaging>.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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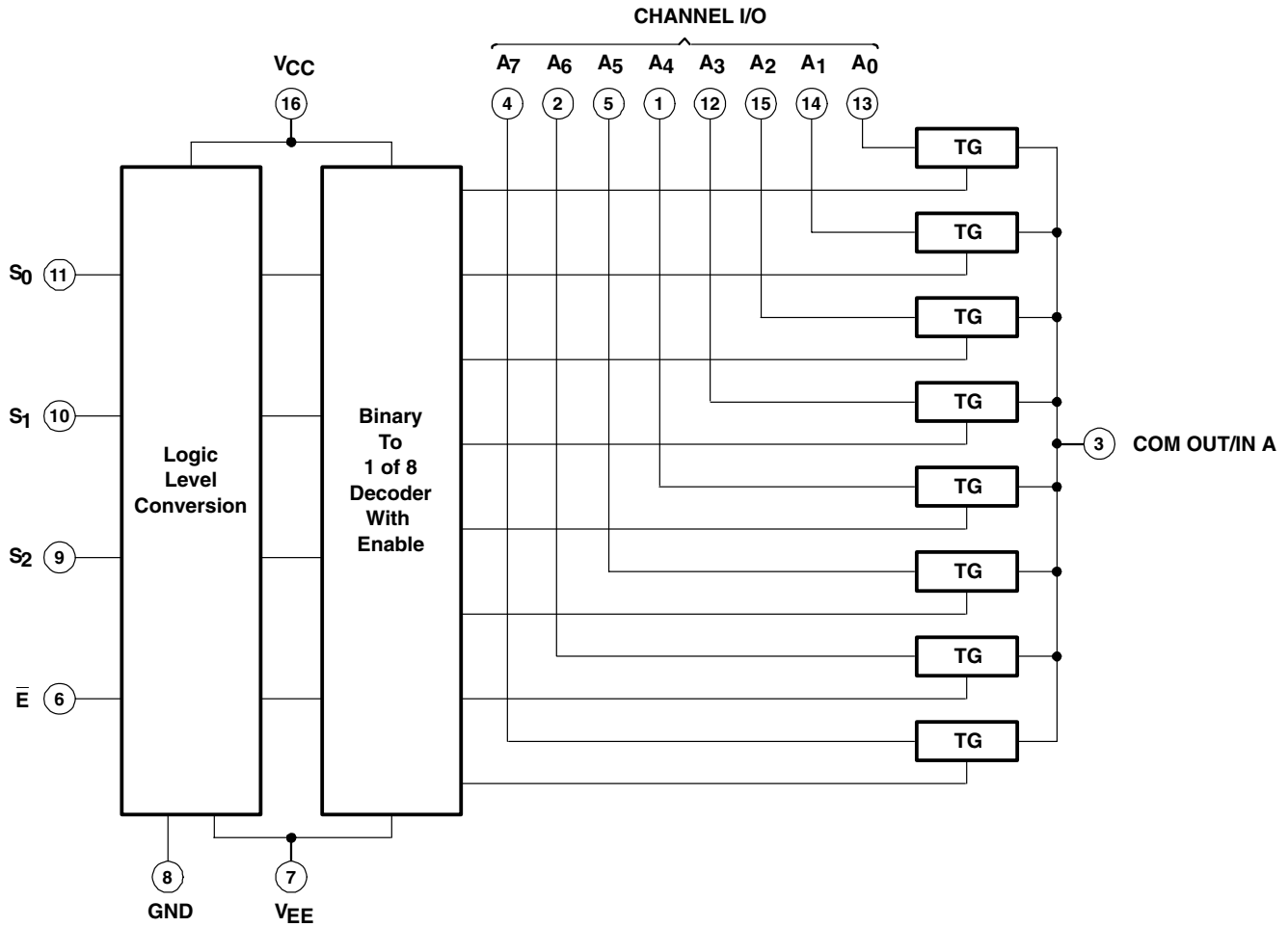
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FUNCTION TABLE

INPUTS				ON CHANNEL(S)
E	S ₂	S ₁	S ₀	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC} - V_{EE}$ (see Note 1)	–0.5 V to 10.5 V
Supply voltage range, V_{CC}	–0.5 V to 7 V
Supply voltage range, V_{EE}	+0.5 V to –7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V)	±20 mA
Output clamp current, I_{OK} ($V_O < V_{EE} - 0.5$ V or $V_O > V_{CC} + 0.5$ V)	±20 mA
Switch current ($V_I > V_{EE} - 0.5$ V or $V_I < V_{CC} + 0.5$ V)	±25 mA
Continuous current through V_{CC} or GND	±50 mA
V_{EE} current, I_{EE}	–20 mA
Package thermal impedance, θ_{JA} (see Note 2): M package	73°C/W
PW package	108°C/W
Maximum junction temperature, T_J	150°C
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ inch ($1,59 \pm 0,79$ mm) from case for 10 s max	300°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT	
V_{CC}	Supply voltage (see Note 4)	2	6	V	
	Supply voltage, $V_{CC} - V_{EE}$ (see Figure 1)	2	10	V	
V_{EE}	Supply voltage, (see Note 4 and Figure 2)	0	–6	V	
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5	V	
		$V_{CC} = 4.5$ V	3.15		
		$V_{CC} = 6$ V	4.2		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V	0.5	V	
		$V_{CC} = 4.5$ V	1.35		
		$V_{CC} = 6$ V	1.8		
V_I	Input control voltage	0	V_{CC}	V	
V_{IS}	Analog switch I/O voltage	V_{EE}	V_{CC}	V	
t_t	Input transition (rise and fall) time	$V_{CC} = 2$ V	0	1000	ns
		$V_{CC} = 4.5$ V	0	500	
		$V_{CC} = 6$ V	0	400	
T_A	Operating free-air temperature	–40	125	°C	

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

4. In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{on} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

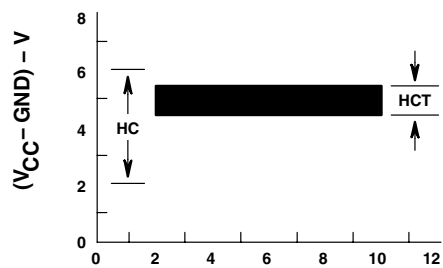


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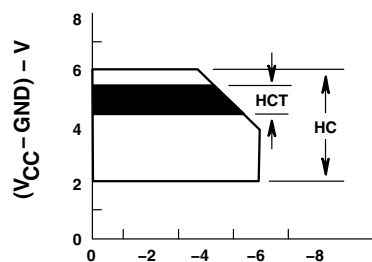
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recommended operating area as a function of supply voltages



(V_{CC} - V_{EE}) - V

Figure 1



(V_{EE} - GND) - V

Figure 2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{EE}	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT	
				MIN	TYP	MAX	MIN	MAX		
r _{on}	I _O = 1 mA, V _I = V _{IH} or V _{IL} , See Figure 8	V _{IS} = V _{CC} or V _{EE}	0 V	4.5 V	70	160	240		Ω	
			0 V	6 V	60	140	210			
			-4.5 V	4.5 V	40	120	180			
		V _{IS} = V _{CC} to V _{EE}	0 V	4.5 V	90	180	270			
			0 V	6 V	80	160	240			
			-4.5 V	4.5 V	45	130	195			
Δr _{on}	Between any two channels	0 V	4.5 V	10					Ω	
		0 V	6 V	8.5						
		-4.5 V	4.5 V	5						
I _{IZ}	For switch OFF: When V _{IS} = V _{CC} , V _{OS} = V _{EE} ; When V _{IS} = V _{EE} , V _{OS} = V _{CC} For switch ON: All applicable combinations of V _{IS} and V _{OS} voltage levels, V _I = V _{IH} or V _{IL}	0 V	6 V	±0.2			±2		μA	
		-5 V	5 V	±0.4			±4			
I _{IL}	V _I = V _{CC} or GND	0 V	6 V	±0.1			±1		μA	
I _{CC}	I _O = 0, V _I = V _{CC} or GND	When V _{IS} = V _{EE} , V _{OS} = V _{CC}	0 V	6 V	8			160		μA
		When V _{IS} = V _{CC} , V _{OS} = V _{EE}	-5 V	5 V	16			320		

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V _{EE}	V _{CC}	T _A = 25°C			T _A = -40°C TO 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t _{pd}	IN	OUT	C _L = 15 pF		5 V	4					ns
			C _L = 50 pF	0 V	2 V	60			90		ns
					4.5 V	12			18		
					6 V	10			15		
-4.5 V	4.5 V			8		12					
t _{en}	ADDRESS SEL or \bar{E}	OUT	C _L = 15 pF		5 V	19					ns
			C _L = 50 pF	0 V	2 V	225			340		
					4.5 V	45			68		
					6 V	38			57		
-4.5 V	4.5 V			32		48					
t _{dis}	ADDRESS SEL or \bar{E}	OUT	C _L = 15 pF		5 V	19					ns
			C _L = 50 pF	0 V	2 V	225			340		
					4.5 V	45			68		
					6 V	38			57		
-4.5 V	4.5 V			32		48					
C _I	Control		C _L = 50 pF					10	10	pF	

operating characteristics, V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER	TYP	UNIT
C _{pd} Power dissipation capacitance (see Note 5)	50	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption, per package.

$$P_D = C_{pd} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_O$$

f_O = output frequency

f_i = input frequency

C_L = output load capacitance

C_S = switch capacitance

V_{CC} = supply voltage

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analog channel characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Switch input capacitance				5		pF
C_{COM}	Common output capacitance				25		pF
f_{max}	Minimum switch frequency response at -3 dB	-2.25 V	2.25 V		145		MHz
		-4.5 V	4.5 V		180		
Sine-wave distortion	See Figure 4	-2.25 V	2.25 V		0.035		%
		-4.5 V	4.5 V		0.018		
\bar{E} or ADDRESS SEL to switch feed-through noise	See Figure 5, and Notes 7 and 8	-2.25 V	2.25 V		(TBD)		mV
		-4.5 V	4.5 V		(TBD)		
Switch OFF signal feed through	See Figure 6 and Figure 10, and Notes 7 and 8	-2.25 V	2.25 V		-73		dB
		-4.5 V	4.5 V		-75		

- NOTES: 6. Adjust input voltage to obtain 0 dBm at V_{OS} for $f_{IN} = 1$ MHz.
 7. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
 8. Adjust input for 0 dBm.

PARAMETER MEASUREMENT INFORMATION

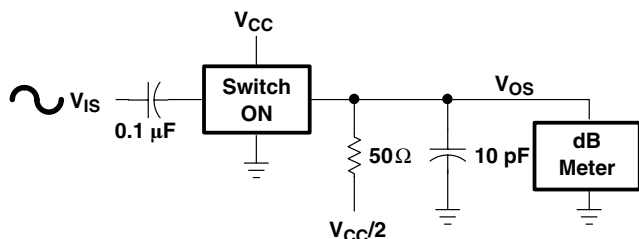


Figure 3. Frequency-Response Test Circuit

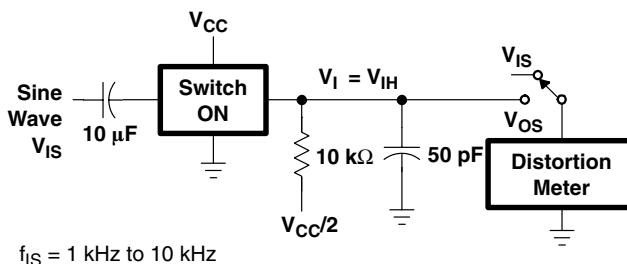


Figure 4. Sine-Wave Distortion Test Circuit

PARAMETER MEASUREMENT INFORMATION

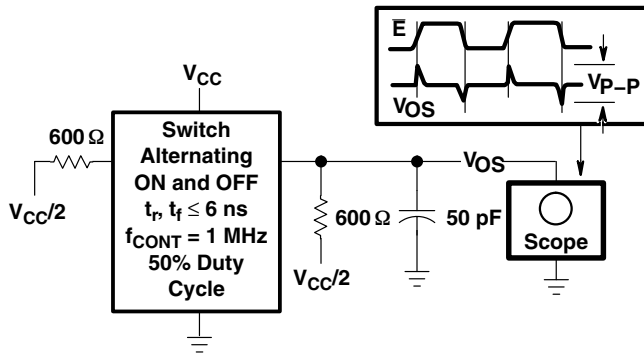


Figure 5. Control to Switch Feedthrough Noise Test Circuit

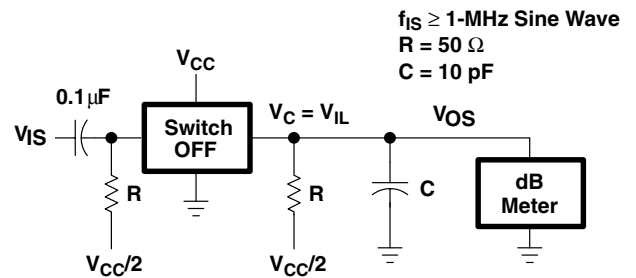
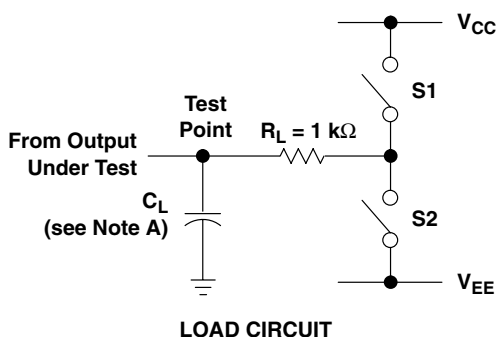


Figure 6. Switch OFF Signal Feedthrough Test Circuit

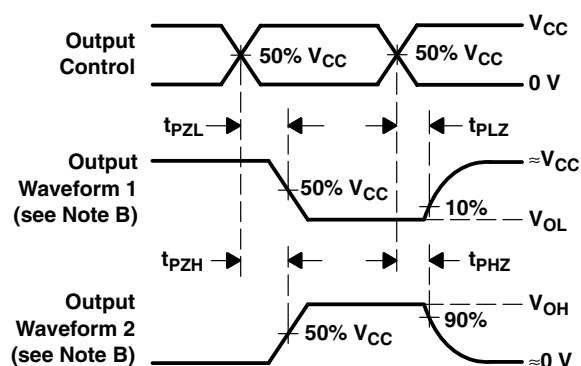
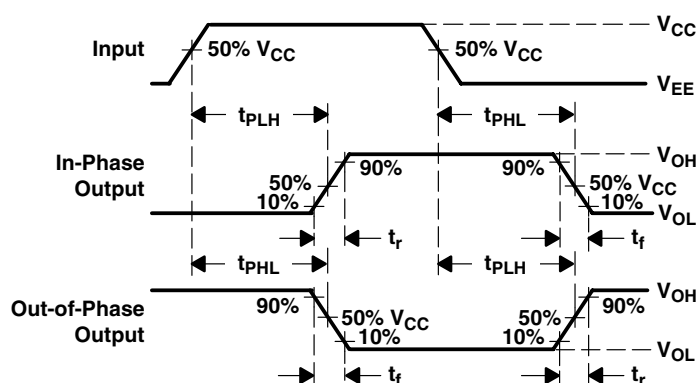
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PARAMETER MEASUREMENT INFORMATION



PARAMETER		S1	S2
t_{en}	t_{pZH}	Open	Closed
	t_{pZL}	Closed	Open
t_{dis}	t_{pHZ}	Open	Closed
	t_{pLZ}	Closed	Open
t_{pd}		Open	Open



- NOTES:
- A. C_L includes probe and test-fixture capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1$ MHz, $Z_O = 50 \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
 - D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
 - E. The outputs are measured one at a time with one input transition per measurement.
 - F. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - G. t_{PZL} and t_{PZH} are the same as t_{en} .
 - H. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 7. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

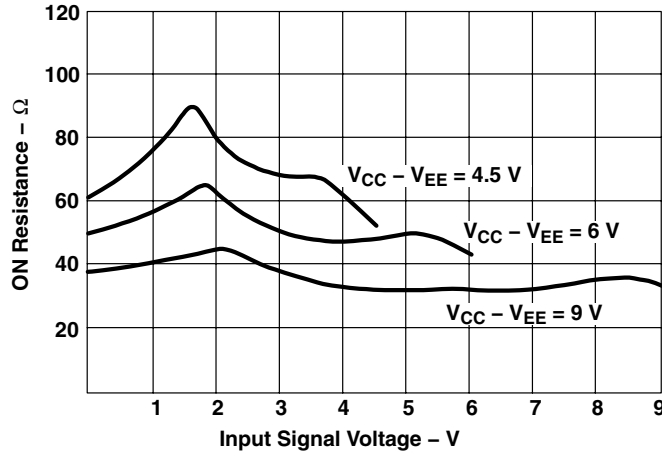


Figure 8. Typical ON Resistance vs Input Signal Voltage

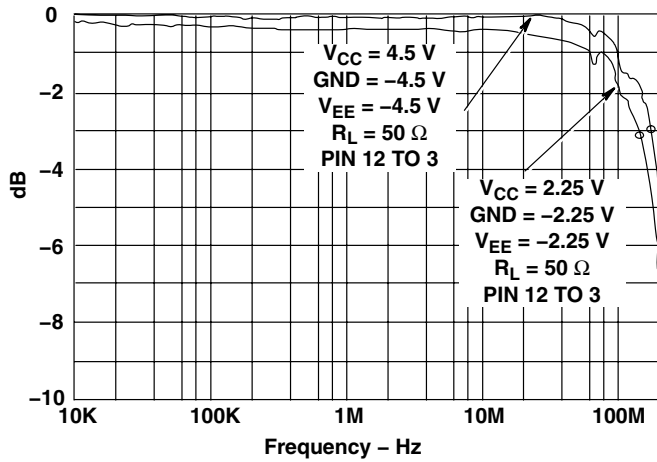


Figure 9. Channel ON Bandwidth

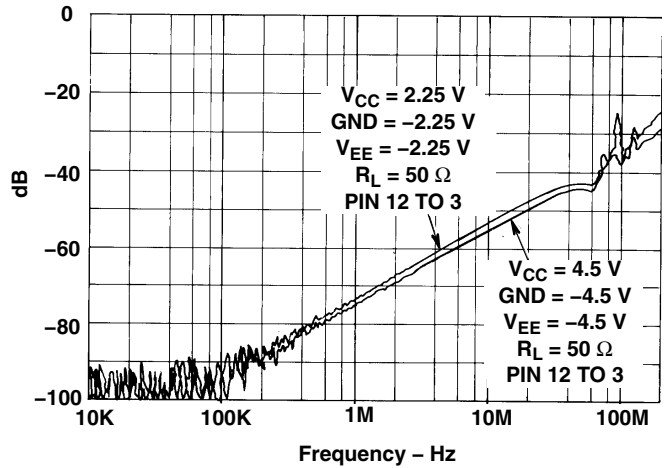


Figure 10. Channel OFF Feedthrough

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4051QM96G4Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q	Samples
CD74HC4051QM96Q1	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HC4051Q	Samples
CD74HC4051QPWRG4Q1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4051Q	Samples
CD74HC4051QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HJ4051Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD74HC4051-Q1 :

- Catalog: [CD74HC4051](#)
- Enhanced Product: [CD74HC4051-EP](#)
- Military: [CD54HC4051](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051QPWRG4Q 1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051QPWRG4Q1	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4051QPWRQ1	TSSOP	PW	16	2000	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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