Triple 3-input NAND gate Rev. 3 — 5 August 2016

Product data sheet

1. **General description**

The 74HC10; 74HCT10 is a triple 3-input NAND gate. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

Features and benefits 2.

- Complies with JEDEC standard JESD7A
- Input levels:
 - For74HC10: CMOS level
 - For 74HCT10: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

Ordering information 3.

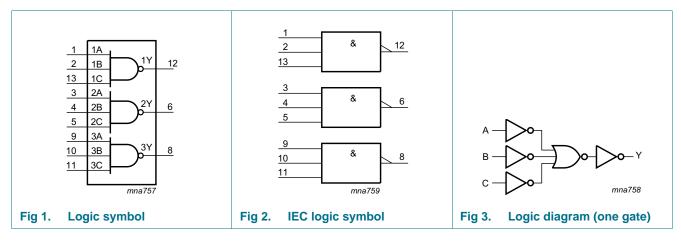
Table 1. **Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74HC10D	–40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCT10D				
74HC10DB	–40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads;	SOT337-1
74HCT10DB			body width 5.3 mm	
74HC10PW	–40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads;	SOT402-1
74HCT10PW			body width 4.4 mm	

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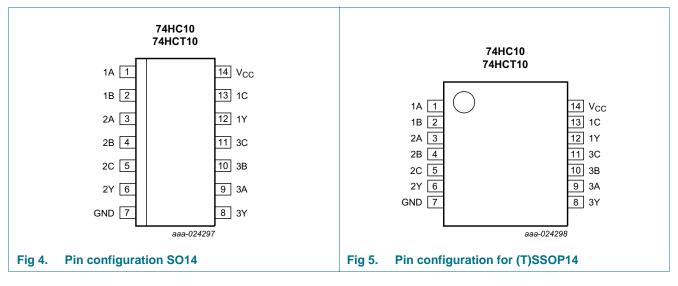
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4. Functional diagram



5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description						
Symbol	Pin	Description				
1A, 2A, 3A	1, 3, 9	data input				
1B, 2B, 3B	2, 4, 10	data input				
GND	7	ground (0 V)				
1C, 2C, 3C	13, 5, 11	data input				
1Y, 2Y, 3Y	12, 6, 8	data output				
V _{cc}	14	supply voltage				

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6. Functional description

Table 3.	Function selection	n[1]		
Input		Output		
nA		nB	nC	nY
L		Х	Х	Н
Х		L	Х	Н
Х		Х	L	Н
Н		Н	Н	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4.Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7	V
I _{IK}	input clamping current	V_{I} < -0.5 V or V_{I} > V_{CC} + 0.5 V	<u>[1]</u>	-	±20	mA
I _{ОК}	output clamping current	$V_{\rm O}$ < –0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	<u>[1]</u>	-	±20	mA
I _O	output current	$-0.5 \text{ V} < \text{V}_{\text{O}} < \text{V}_{\text{CC}} + 0.5 \text{ V}$		-	±25	mA
I _{CC}	supply current			-	50	mA
I _{GND}	ground current			-50	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	SO14 and (T)SSOP14	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 $^\circ\text{C}.$

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter Conditions		74HC10			74HCT			Unit
			Min	Тур	Max	Min	Тур	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C
$\Delta t / \Delta V$	input transition rise and fall rate	$V_{CC} = 2.0 V$	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5 V$	-	1.67	139	-	1.67	139	ns/V
		$V_{CC} = 6.0 V$	-	-	83	-	-	-	ns/V

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9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C t	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HC10	1	1								
VIH	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
	V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V	
VIL	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_I = V_{IH} \text{ or } V_{IL}$								
	output voltage	I_{O} = -20 μ A; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
	$I_O = -20 \ \mu\text{A}; \ V_{CC} = 4.5 \ \text{V}$	4.4	4.5	-	4.4	-	4.4	-	V	
		$I_{O} = -20 \ \mu A; \ V_{CC} = 6.0 \ V$	5.9	6.0	-	5.9	-	5.9	-	V
		I_{O} = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_{O} = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}$								
	output voltage	$I_{O} = 20 \ \mu A; \ V_{CC} = 2.0 \ V$	-	0	0.1	-	0.1	-	0.1	V
		I_{O} = 20 μ A; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		$I_{O} = 20 \ \mu A; V_{CC} = 6.0 \ V$	-	0	0.1	-	0.1	-	0.1	V
		I_{O} = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_{I} = V_{CC} \text{ or GND};$ $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current		-	-	2.0	-	20	-	40	μΑ
CI	input capacitance		-	3.5	-	-	-	-	-	pF

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Symbol	Parameter	Conditions		25 °C		–40 °C t	o +85 °C	–40 °C to	o +125 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT1	D									
V _{IH}	HIGH-level input voltage	$V_{CC} = 4.5 V \text{ to } 5.5 V$	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
	I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V	
V _{OL}	LOW-level output voltage	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
		$I_{O} = 20 \ \mu A; V_{CC} = 4.5 \ V$	-	0	0.1	-	0.1	-	0.1	V
		$I_0 = 4 \ \mu A; \ V_{CC} = 4.5 \ V$	-	0.15	0.26	-	0.33	-	0.4	V
lı	input leakage current		-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$\label{eq:VI} \begin{array}{l} V_{I} = V_{CC} \text{ or } GND; \ I_{O} = 0 \ A; \\ V_{CC} = 5.5 \ V \end{array}$	-	-	2.0	-	20	-	40	μA
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A};$ other inputs at V_{CC} or GND; $V_{CC} = 4.5 \text{ V}$ to 5.5 V	-	150	540	-	675	-	735	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $GND = 0 V; C_L = 50 pF;$ for test circuit, see <u>Figure 7</u>.

Symbol	Parameter	Conditions	Conditions		25 °C		–40 °C to +125 °C		Unit
				Min	Тур	Мах	Max (85 °C)	Max (125 °C)	
74HC10		·							
t _{pd} propagation delay		nA, nB to nY; see <u>Figure 6</u>	<u>[1]</u>						
		V _{CC} = 2.0 V		-	30	95	120	145	ns
	$V_{CC} = 4.5 V$		-	11	19	24	29	ns	
		$V_{CC} = 5.0 \text{ V}; \text{ C}_{L} = 15 \text{ pF}$		-	9	-	-	-	ns
		$V_{\rm CC} = 6.0 \ V$		-	9	16	20	25	ns
t _t	transition time	see <u>Figure 6</u>	[2]						
		V _{CC} = 2.0 V		-	19	75	95	110	ns
		$V_{CC} = 4.5 V$		-	7	15	19	22	ns
		V _{CC} = 6.0 V		-	6	13	16	19	ns
C _{PD}	power dissipation capacitance	per package; $V_I = GND$ to V_{CC}	<u>[3]</u>	-	12	-	-	-	pF

Triple 3-input NAND gate

Symbol Parameter Conditio		Conditions		25 °C			-40 °C to	Unit	
			Min		Тур	Max	Max (85 °C)	Max (125 °C)	_
74HCT10)	1							
t _{pd}	propagation delay	nA, nB to nY; see Figure 6	<u>[1]</u>						
		V _{CC} = 4.5 V		-	14	24	30	36	ns
		V _{CC} = 5.0 V; C _L = 15 pF		-	11	-	-	-	ns
t _t	transition time	V _{CC} = 4.5 V; see <u>Figure 6</u>	[2]	-	7	15	19	22	ns
C _{PD}	power dissipation capacitance	per package; V _I = GND to V _{CC} – 1.5 V	<u>[3]</u>	-	14	-	-	-	pF

Table 7. Dynamic characteristics ... continued GND = 0 V: $C_{i} = 50$ pF: for test circuit, see Figure 7.

 $\label{eq:tpd} [1] \quad t_{pd} \text{ is the same as } t_{PHL} \text{ and } t_{PLH}.$

- [2] t_t is the same as t_{THL} and t_{TLH} .
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μ W):

 P_{D} = $C_{PD} \times V_{CC}{}^{2} \times f_{i} \times N$ + \sum ($C_{L} \times V_{CC}{}^{2} \times f_{o}$) where:

 f_i = input frequency in MHz;

 $f_o = output frequency in MHz;$

 C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V;

N = number of inputs switching;

 Σ (C_L × V_{CC}² × f_o) = sum of outputs.

11. Waveforms

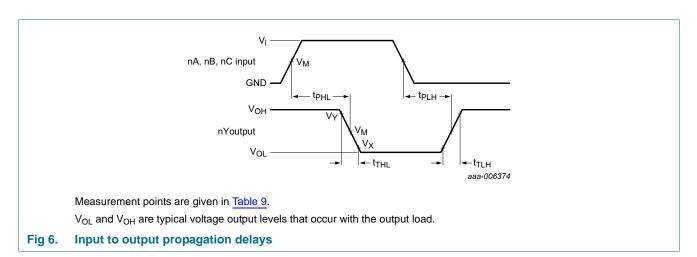


Table 8. Measurement points

Туре	Input	Output			
	V _M	V _M	V _X	V _Y	
74HC10	0.5V _{CC}	0.5V _{CC}	0.1V _{CC}	0.9V _{CC}	
74HCT10	1.3 V	1.3 V	0.1V _{CC}	0.9V _{CC}	

74HC_HCT10 Product data sheet

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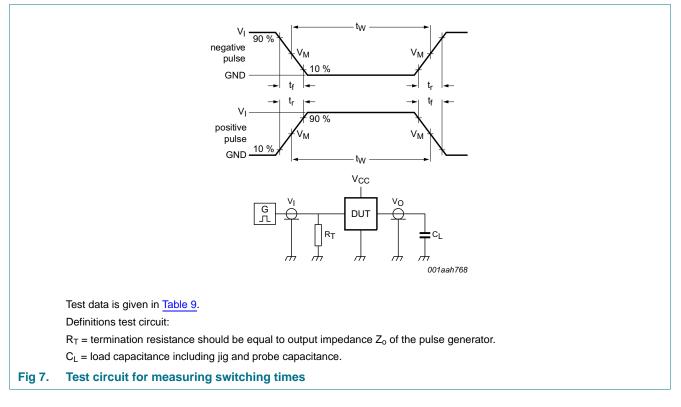


Table 9. Test data

Туре	Input L		Load	Test
	VI	t _r , t _f	CL	
74HC10	V _{CC}	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT10	3.0 V	6.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

Triple 3-input NAND gate

12. Package outline

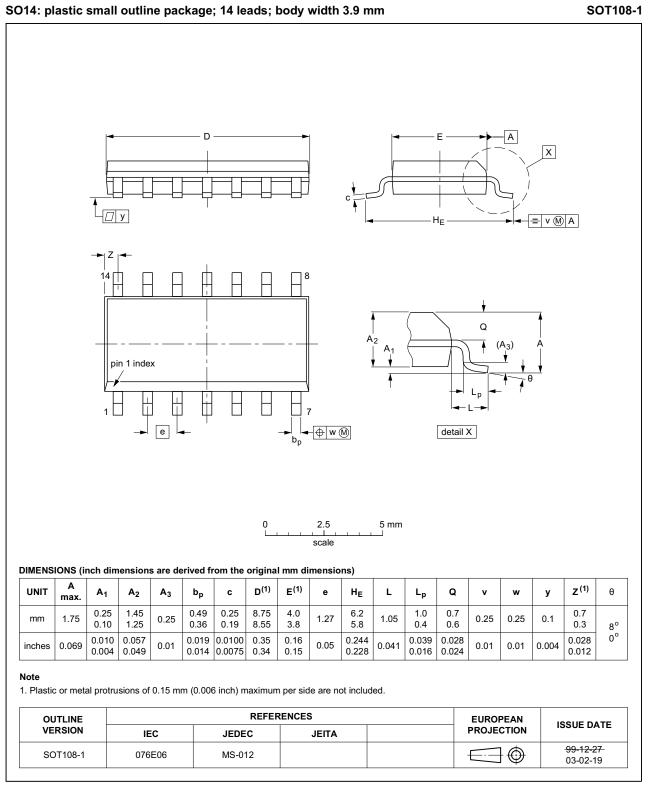


Fig 8. Package outline SOT108-1 (SO14)

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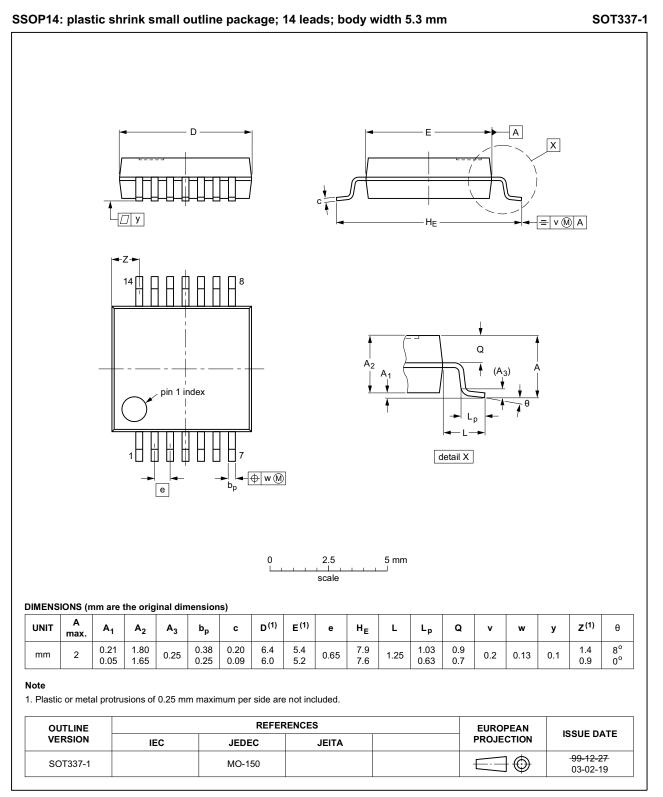


Fig 9. Package outline SOT337-1 (SSOP14)

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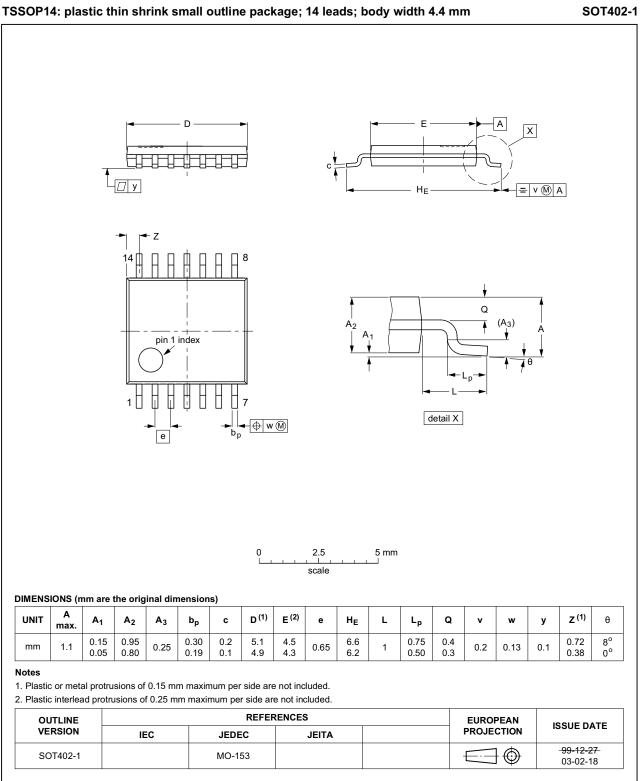


Fig 10. Package outline SOT402-1 (TSSOP14)

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Triple 3-input NAND gate

13. Abbreviations

Table 10. Abbreviations					
Acronym	Description				
CMOS	Complementary Metal-Oxide Semiconductor				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
НВМ	Human Body Model				
MM	Machine Model				
TTL	Transistor-Transistor Logic				

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT10 v.3	20160805	Product data sheet	-	74HC_HCT10_CNV v.2
Modifications:	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. 			
	 Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT10_CNV v.2	19901201	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions"

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